Enhancing SRAM Efficiency: A Novel Approach Utilizing Majority Gate Technology in CMOS 7 nm Design

Akula Mallaiah[a)], Sai Sanjana Kasturi Kammela[b)], Naga Sai Deepika Motamarri [c)], Chanikya Madhav Golla[d)], Siva Bharath Lukka[e)]
Department of Electronics and Communication Engineering,
SR Gudlavalleru Engineering College, Gudlavalleru, Andhra Pradesh, India.

ABSTRACT:

To meet the increasing demands of modern devices, extensive memory capacities are now standard. Key performance metrics such as area, delay, and power consumption play crucial roles in determining device efficiency. For years, Random-Access Memory (SRAM) has been a prevalent memory technology, offering flexible data storage capabilities. Utilizing latching circuitry, SRAM maintains data bits with the assistance of MOSFETs, highlighting the importance of enhancing System on Chip (SoC) capabilities.

This study focuses on optimizing the competitive performance of Static Random Access Memory (SRAM) by reducing delay and transistor count, thereby minimizing area requirements. By employing CMOS transistors in the design architecture of Random-Access Memory, the aim is to achieve reduced size and area for improved delay characteristics in CMOS 7 nm technology. The design methodology is rooted in majority logic, serving as the foundational element for the entire system. The memory cell design, a core component of low-power Random Access Memory systems, is tailored to efficiently store a nibble of data.

Leveraging DSCH tool 3.9 for generating an efficient memory design and Micro wind tool 3.9 for evaluating circuits in CMOS 7 nm technology, this study showcases comparisons in power dissipation, area, and power delay product. The proposed design approach is simulated using Micro wind 3.9 in the context of 7 nm CMOS technology, demonstrating its potential for enhanced memory system performance. The proposed majority logic based SRAM design achieves nearly 97% of less delay when compared to other designs.

Keywords: Majority gate, SRAM, DSCH, Micro wind

INTRODUCTION:

The increasing demand for low-power circuits is driven by the proliferation of battery-operated portable consumer devices. The quest for reduced power consumption aligns with the desire for lighter, smaller, and more durable electronic gadgets, where battery life is a critical factor. The surge in consumer electronics like mobile phones, laptops, and portable systems has spurred research efforts in low-power microelectronics. The focus on low power is paramount for enhancing the performance of these consumer systems, reflecting evolving consumer preferences.

Over the past four decades, CMOS devices have undergone significant size reductions to enhance speed, performance, and decrease power consumption. SRAM plays a vital role in low-power VLSI devices, particularly in high-speed applications such as buffers and caches. Unlike DRAM, which uses capacitors, SRAM's transistor-based design offers faster operation, making it ideal for high-speed memory applications. Technological advancements have enabled the integration of millions of transistors on a single chip, revolutionizing chip design capabilities.

This paper aims to design an efficient 4 x 4 Random Access Memory utilizing 7 nm CMOS technology. Central to this design is the memory cell, implemented using majority logic. The proposed designs emphasizes efficiency in terms of read and write operation delays in the RAM cell, aligning with the objective of optimizing performance while minimizing power consumption.

RELATED WORK:

Hans Raj et al [1] showcased a novel SRAM cell design tailored for low power consumption in consumer devices such as mobile phones and laptops. The design approach focused on evaluating the area and power requirements of individual transistors within the cell, leading to substantial enhancements in overall efficiency and performance.

P. Sri Charan et.al [2] introduced the Self Voltage Level (SVL) technique. The mplementation of an SVL circuit in a 7T SRAM cell showcased a significant reduction in leakage compared to a standard 7T SRAM cell. While this led to a slight increase in the cell's area, the lower current leakage achieved through this technique resulted in reduced power consumption.

Radhika Chandak et.al[3] presented a study on the development of a 256-bit SRAM utilizing various CMOS technologies. The analysis included parameters such as power dissipation,

delay, and area for each technology. However, the study did not specifically address an optimized design strategy for handling larger bit capacities simultaneously.

Akshay Bhaskar et.al [4] introduced a low-power SRAM cell design and analysis. The study evaluated two power reduction techniques, namely Gated VDD and MTCMOS-based designs, in the context of 90nm technology. While these techniques showed improvements over traditional designs, they were found to be inadequate for handling multiple bits simultaneously.

Sandeep R et.al [5] examined the implementation of a 4T SRAM cell utilizing submicron CMOS technology. While the suggested design demonstrated lower power consumption compared to traditional designs, a notable limitation was observed in terms of increased area requirements. This was primarily due to the necessity of a higher number of transistors in the proposed design.

PROBLEM STATEMENT:

The design of SRAM cells, commonly found in devices like phones and laptops, has traditionally relied on CMOS technology [6]. However, this approach has drawbacks such as high power consumption, increased chip space utilization, and relatively slower memory operations [8]. To address these issues, we propose a novel technology known as Majority Gate technology. Our aim is to demonstrate how Majority Gate technology can mitigate the limitations associated with CMOS technology by offering reduced power consumption, optimized chip space utilization, and enhanced speed performance. In essence, our project focuses on exploring a new and improved method for creating computer memory that enhances the efficiency of our devices [7]. We are enthusiastic about the potential benefits that Majority Gate technology can bring and believe it has the capability to overcome the challenges posed by current CMOS-based memory design technologies.

PROPOSED MODULE DESIGN

This flowchart outlines a comprehensive procedure for designing a Static Random Access Memory (SRAM) cell utilizing majority gate technology. It involves utilizing the DSCH software for generating schematic designs and the Micro wind software for compiling Verilog files and conducting analysis. The flowchart serves as a guide for designers, assisting them in successfully designing efficient SRAM cells with majority gate technology. The step-by-step

methodology presented in the flowchart facilitates the creation of dependable SRAM cells using majority gate technology.

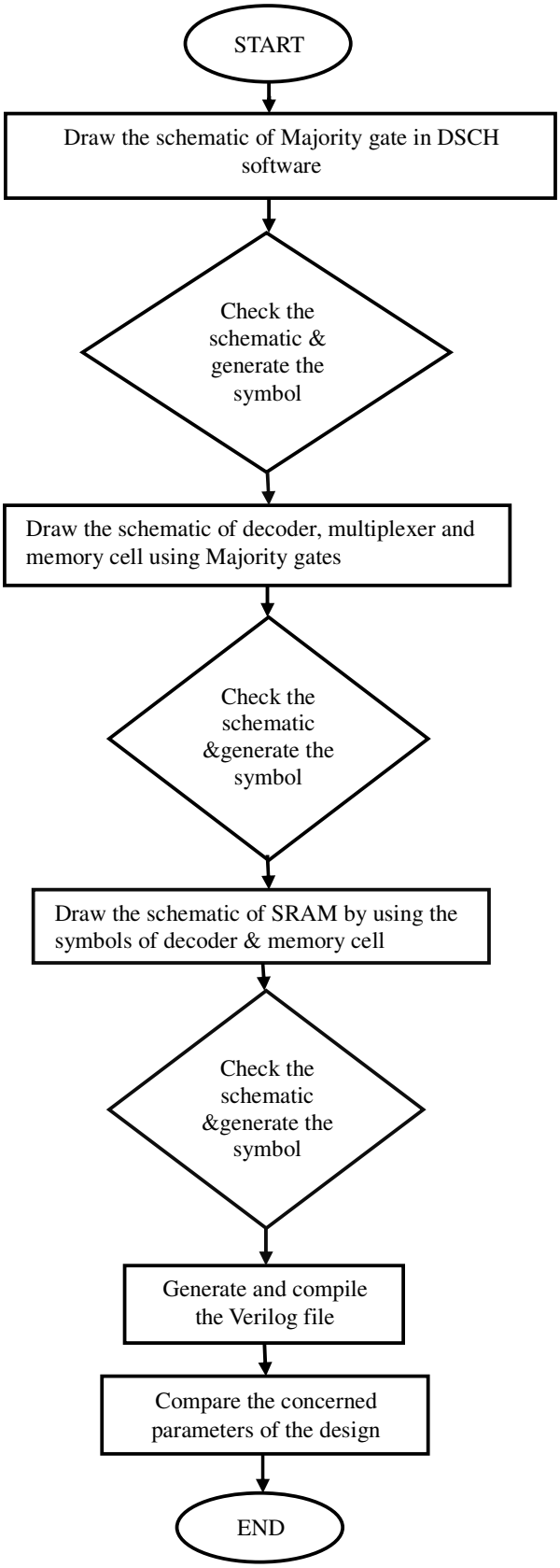

Figure 1: Design flow of 4x4 SRAM Cell

In the proposed design, an efficient 4x4 RAM was developed using optimized CMOS technology known as majority gate technology. The design process involved creating a schematic for the majority gate using DSCH software, verifying for errors, and saving the symbol for future use. A Verilog file was generated in DSCH, compiled in Microwind to produce the majority gate layout. Using the majority gate symbol, schematics for the decoder, multiplexer, and memory cell were designed, and symbols were generated for each component. The schematic for the SRAM cell was created using these symbols, errors were checked, and the symbol was generated. The schematic was run to extract the truth table, and a Verilog file was made in DSCH, compiled in Microwind to check for errors and generate the layout. Finally, simulations were conducted to compare power, delay, and area parameters with traditional CMOS technology.

The below figure 2 depicts the circuit-level representation of the Majority gate using CMOS technology. Our design, featuring 3 PMOS and 3 NMOS transistors, demonstrates superior efficiency compared to alternative designs employing 6 PMOS and 6 NMOS transistors. By optimizing transistor count without compromising functionality, we achieve streamlined circuitry, reducing both resource consumption and manufacturing complexity while maintaining performance standards.

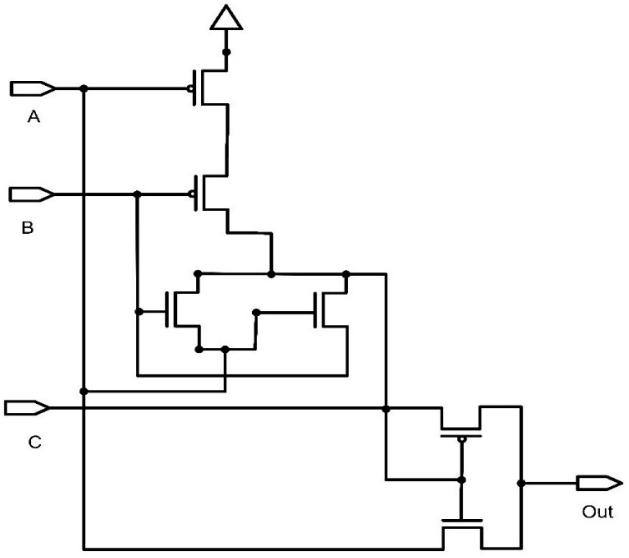

Figure 2: Circuit Diagram of Majority Gate

The below figure 3 depicts the circuit-level representation of 4x4 SRAM Cell. In our 4x4 SRAM design, we utilize majority gate technology, which employs fewer transistors compared to traditional CMOS-based SRAM cells. This design utilizes 16 memory cells for storing a nibble at a time. Each cell in our design consists of majority gates for both the bit line and word line access, resulting in a simpler and faster circuit.

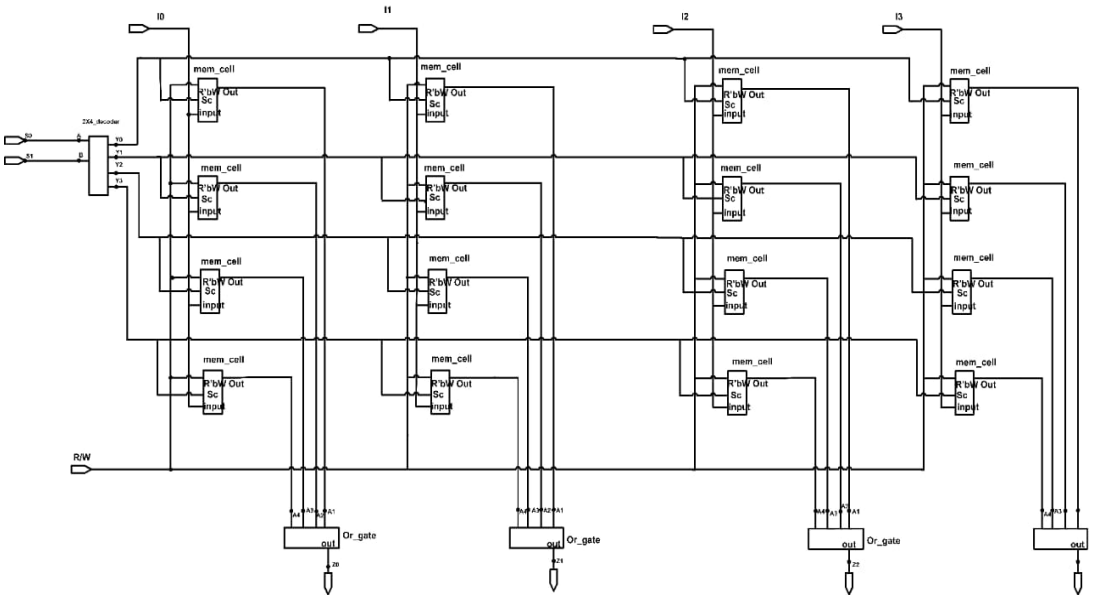

Figure 3: Circuit Diagram of 4x4 SRAM Cell

SIMULATION RESULTS

The simulation circuit of the Majority gate designed using DSCH software is depicted in Figure 4. Its remarkable performance metrics include a power consumption of 623nW and a total area of 7.4 μm^2. Moreover, the gate exhibits an impressively low delay of 0.00325ns, approximately 98% less than that obtained in [9]. Within the DSCH software, the operation of the Majority gate has been thoroughly verified for all input combinations, ensuring its reliability and functionality across diverse scenarios.

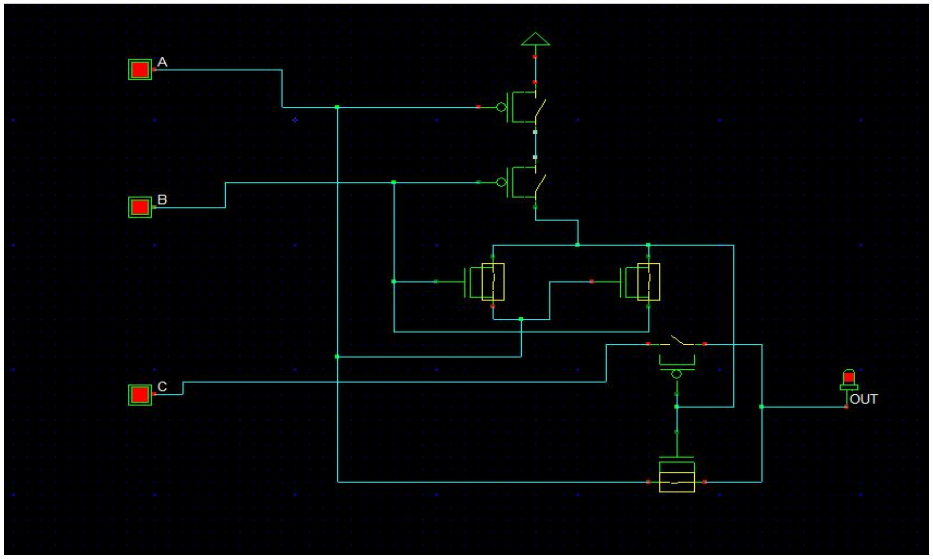

Figure 4: DSCH majority gate design

The SRAM cell's simulation circuit created using DSCH software and depicted in Figure 5, showcases notable performance metrics. These metrics include a power consumption of 764.408 μW and a total area of 215.9 μm^2. Additionally, the SRAM cell demonstrates an impressively short delay of 51.2ps, which is about 97% less than that reported in [5]. Through comprehensive verification in the DSCH software, the SRAM cell's functionality across various input combinations is confirmed, ensuring its reliability across different scenarios.

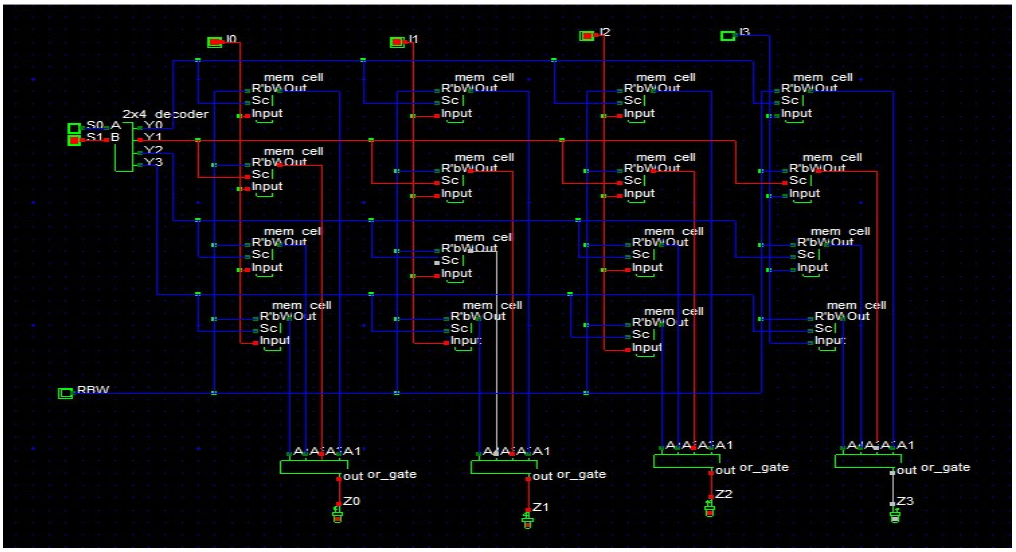

Figure 5: DSCH 4x4 SRAM cell design

The timing diagrams of the majority gate and proposed SRAM cell in DSCH software are presented in Figure 6 and Figure 7 respectively. These timing diagrams depict the working of the majority gate and SRAM cell for all input combinations.

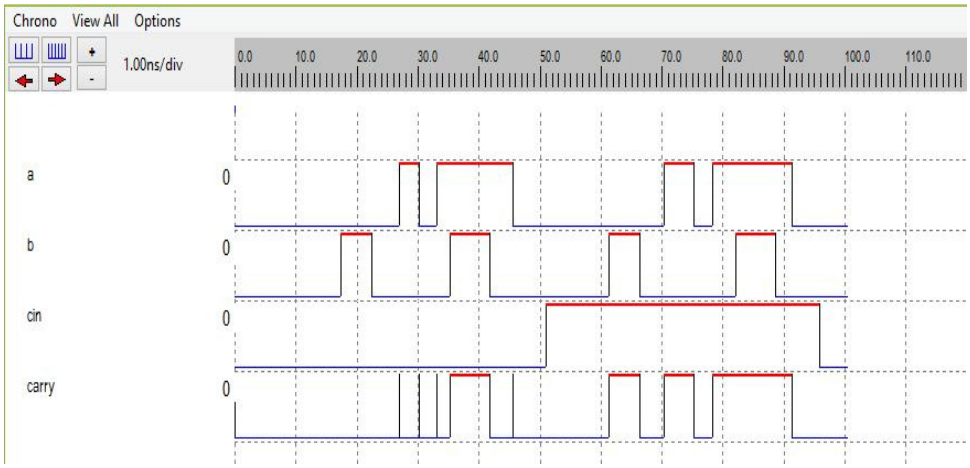

Figure 6: Timing Diagram of DSCH Majority gate Design

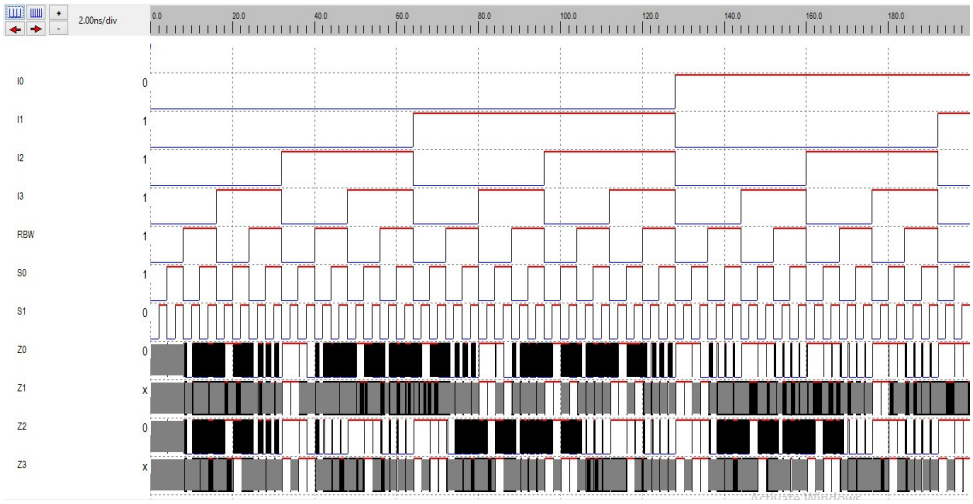

Figure 7: Timing Diagram of Proposed DSCH 4x4 SRAM Cell

The layout of the majority gate is executed in 7nm technology using the Micro wind tool 3.9 for area and delay assessment, as illustrated in Figure 8. The area of the layout of majority gate in 7 nm technology is found to be 7.4 μm^2.

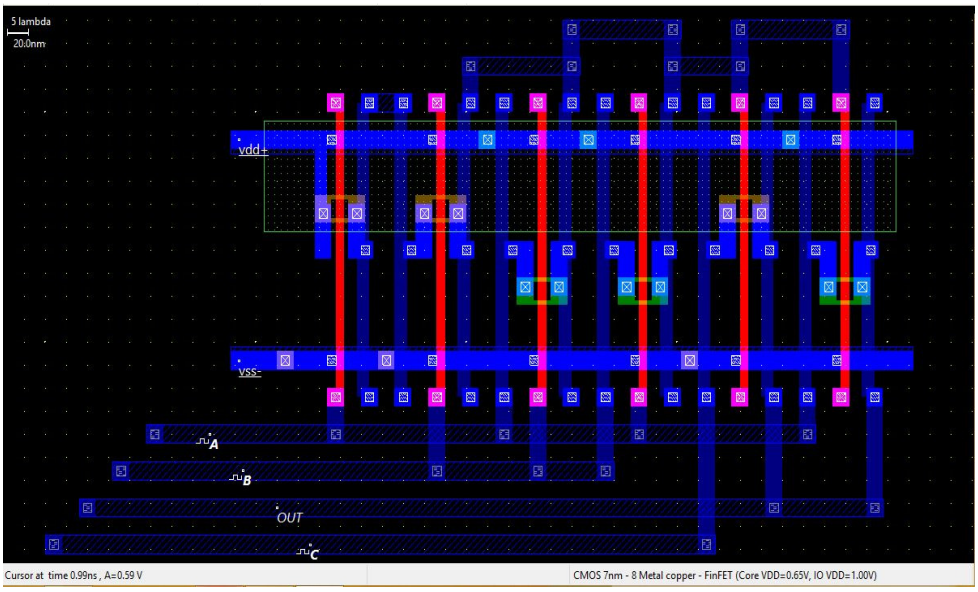

Figure 8: Layout of majority gate in Microwind

The layout of the proposed SRAM cell design is executed in 7nm technology using the Micro wind tool 3.9 for area and delay assessment, as illustrated in Figure 9. The design of the 4x4 SRAM is conducted in 7nm technology and the area of the 4x4 SRAM cell layout is found to be 215.9 μm^2.

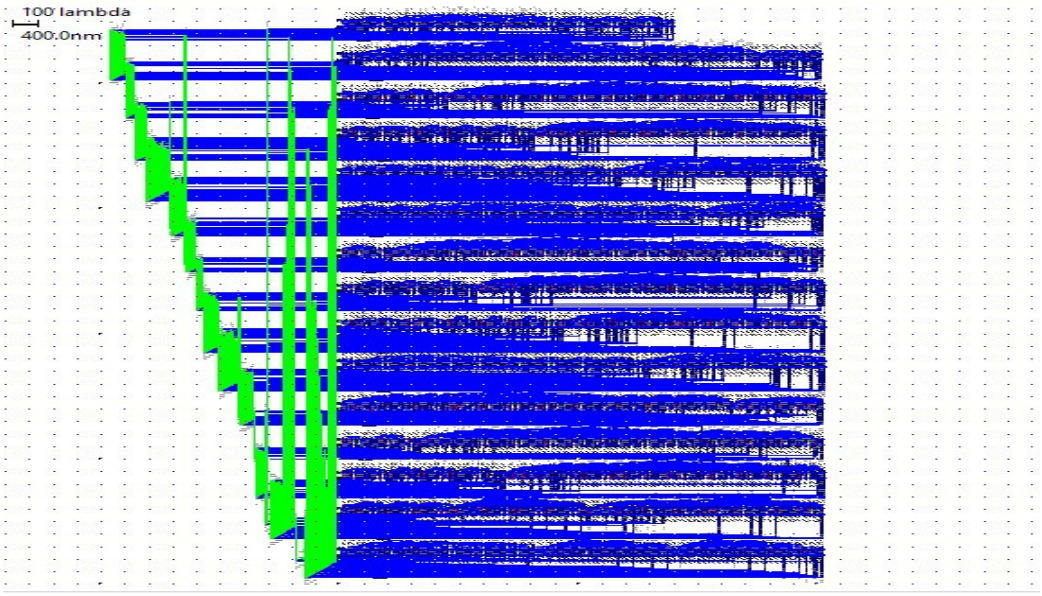

Figure 9: Layout of proposed 4x4 SRAM cell in Microwind

The following table depicts the comparison of parameters such as area, power, and delay of the proposed SRAM cell with various existing works.

Table 1: Comparison of our design with the existing works.

Design (size)	**Properties**			
	Tech.	**Area**	**Power**	**Delay**
Low power SRAM [1] (2x1)	CMOS	-	606.519nW	-
RAM [10] (4x1)	Quantum Dot	0.12 μm^2	-	-
4T SRAM [5] (1x1)	Deep Submicron CMOS	-	18.9 µW	2077.6 ps
3T SRAM [16] (2x1)	CMOS	-	1.91 µW	-
This Work (4x4)	Majority gate - CMOS	215.9 μm^2	764.408µW	51.2ps

CONCLUSION:

In conclusion, our paper introduces a novel technology known as Majority Gate, which has the potential to revolutionize the way we design memory for devices such as phones and laptops. Our objective was to address the shortcomings associated with current CMOS technology, including high power consumption, large chip space requirements, and relatively slower performance. Through our investigation, we have discovered that Majority Gate technology presents solutions to these challenges.

In summary, the paper aimed at designing an efficient 4x4 SRAM utilizing CMOS 7nm technology has successfully achieved its objectives. The SRAM cell demonstrates promising performance metrics, with an area footprint of 215.9µm², a minimal delay of 51.2ps which is found to be 97% less than the existing work, and a power consumption of 764.08µW. These results underscore the feasibility and effectiveness of the proposed design in meeting the demands of modern semiconductor applications.

REFERENCES:

[1] Hansraj, Alka Chaudhary, Ajay Rana, Ultra Low power SRAM Cell for High Speed Applications using 90nm CMOS Technology, ICRITO, June 4-5, 2020.

[2] P. Sri Charan, N. Sai Deepak, Vemula Panduranga, Design and Implementation of CMOS based SRAM Memory Array using SVL Technique at 28nm Technology, International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181 IJERTV11IS050223 Vol. 11 Issue 05, May-2022.

[3] Radhika Chandak, Implementation of 256 bit SRAM by using 45nm and 90nm technologies in Microwind, International Research Journal of Engineering and Technology (IRJET), Volume: 07 Issue: 06, June 2020.

[4]Akshay Bhaskar**,** Design and analysis of low power SRAM cell, April 2017 DOI:10.1109/ IPACT.2017.8244888.

[5] Sandeep R, Narayan T Deshpande, A R Aswatha, Design and Analysis of a New Loadless 4T SRAM Cell in Deep Submicron CMOS Technologies, ICETET-09.

[6] Senthil Kumaran Varadharajan, Low Power VLSI circuits design Strategies and methodologies, 2017.

[7] V. Rukkumani Nanjundappa, Devarajan, Design of low power writes driver circuit for 10t SRAM cell, January 2015.

[8] G. Pasandi and S. M. Fakhraie, "A New Sub-Threshold 7T SRAM Cell Design with Capability of Bit-Interleaving in 90 nm CMOS," in Proc.21st ICEE, Mashhad, 2013, pp. 1–6.

[9] Wael Saad Ahmed, Nabeel Abdulrazaq yaseen, Nsaif Jasim Al Chaabawi, “Design, Simulation and Investigation of Basic Logic Gates by using Nand Logic Gate”, 10.1063/5.0119320, March 2023.

[10] M.Azath, Dr. Jayabrabu Ramakrishnan, Omer Tayfour, “A new efficient design for Random Access Memory based on Quantum Dot Cellular Automata Nano Technology”, Elseiver, 2019.

[11] Yen Hsiang Tseng, Yimeng Zhang, Leona Okamura, and Tsutomu Yoshihara, A New 7t SRAM cell design with high read stability, IEEE 4244-6632, 2010.

[12] N. K. Khokhara and B. H. Nagpara, “Design and Performance Analysis of 256 bit SRAM Using different SRAM cell in 45nm CMOS Technology”, Int. J. Mod. Trends Eng. Res., vol. 4, no. 3, pp. 216–222, April 2017.

[13] M. Devi, C. Madhu, and N. Garg, “Design and analysis of CMOS based 6T SRAM cell at different technology nodes”, Mater. Today Proc., vol. 28, pp. 1695–1700, 2020, doi: 10.1016/j.matpr.2020.05.130.

[14] Nuaomi Jusat and Ahmad Anwar Zainuddin, “Design and Optimization of 4-BIT Static RAM and 4-BIT Dynamic RAM for Compact and Portable Devices ”, Malaysian J. Sci. Adv. Tech., vol. 1, no. 3, pp. 97–102, Jul. 2021.

[15] Divya & Rawat, Bhawna, Design and Performance Analysis of High-Performance Low Power Voltage Mode Sense Amplifier for Static RAM, 20. 10.15598/aeee.v20i3.4373, 2022.

[16] Velguri Suresh Kumar, Maturi Sarath Chandra, Jupudi VamsiKrishna, “Design and Implementation of Three Transistor SRAM Cell using 45nm CMOS Technology”, DOI: 10.1109/ICISS49785.2020.9316122.

[17] Divya Dutt, Poornima Mittal, Bhawna Rawat, Brijesh Kumar, “Design and Performance Analysis of High-Performance Low Power Voltage Mode Sense Amplifier for Static RAM”, DOI: 10.15598/aeee.v20i3.4373, September 2022.

[18] B. K. L. Aruna and D. Sravani, 'Design of 21t Sram Cell for Low Power Applications', Int. J. Innov. Technol. Explor. Eng., vol. 8, no. 9, pp. 2523–2527, Jul. 2019, doi: 10.35940/ijitee.H7148.078919.

[19] B. Kaleeswari and S. Kaja Mohideen, 'Design, Implementation and Analysis of 8T SRAM Cell in Memory Array', Int. J. Eng. Technol., vol. 7, no. 3.1, p. 101, Aug. 2018, doi: 10.14419/ijet.v7i3.1.16808.

[20] R. Kataria, Priya, Neeharika, Design And Performance Analysis of 6T SRAM cell at 90nm Technology, Int. J. Adv. Res. Electron. Commun. Eng. 5 (2016) 984– 987.

[21] C.A. Kumar, B.K. Madhavi, K. Lalkishore, Performance analysis of low power 6T SRAM cell in 180nm and 90nm, in: 2016 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and BioInformatics (AEEICB), IEEE, 2016, pp. 351–357.

[22] Sayeed Ahmad, Mohit Kumar Gupta, Naushad Alam and Mohd. Hasan “Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell”, IEEE transactions on very large scale integration (Vlsi) systems 2016.

[23] Neelam Surana, Joycee Mekie “Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications”, IEEE Transactions on Circuits and Systems II, 2018.