HIGH-SPEED COUNTER WITH NOVEL LFSR STATE EXTENSION

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Abstract

In conjunction with a unique LFSR state extension, this work proposes a high-speed counter design. The proposed state extension is used to expand an m-bit LFSR calendar of (2m -1) states to 2m states without reducing the counting rate. The suggested counter comprises two sub-counters that achieve a high collecting rate and minimise the hardware complexity required to convert an LFSR phase into a binary state. This counter is based on the idea as merely the low-order bytes are swapped often. The low-order sub-counter is designed using the proposed LFSR counter, and the high-order sub-counter is designed using the conventional synchronous binary counter. Moreover, the counter constructed takes into consideration the speed drop caused by the large fan-out of the high order sub-counter. Xilinx ISE/Vivado tools were used to design the suggested counter using Verilog HDL.

Key Words : Arithmetic and logic units, combinational logic, high-speed arithmetic, sequential circuits

1. INTRODUCTION

Demand for broad bit-width, high-speed counters has been rising recently for a variety of applications, including phase-locked loops, frequency synthesizers, and time-to-digital converters (ADCs and TDCs). The traditional binary counter cannot attain an increased calling rate even though the counter gets small enough since competing against each other are the counter size and the counting rate. Furthermore, in order to achieve a consistent clock rate regardless of the counter size, Since the counter size influences the adder's latency, most synchronous basic counts that involve an addition function or an idle register are ineffective. Since the counter size influences the adder's latency, most synchronous basic counts that involve an addition function or an idle register are ineffective. A status generator can be used to create a time-keeping synchronous counter when the binary value is not needed right away. A popular state generator is a nonlinear feedback slip register (LFSR), which uses a feedback connection to determine the future state from the current one.

Given that the LFSR's delay is essentially independent of size and that it can be implemented using merely D switched-flop (F/Fs) & exclusive-OR (XOR) gates, It can be utilised to create a synchronous counter with a high speed and consistent time. There are two types of with varying feedback connections between LFSR. One LFSR is many-to-one, meaning that numerous F/Fs are needed to create a single feedback value. & the remainder is an one-to-man LFSR, in which numerous F/Fs receive a single F/F value. As the quantity of input bits involved in the feedback rises, Similar to a binary counter, the many-to-one LFSR's operating speed drops. However, a lot of earlier research has utilised a multiple Without considering the difference in speed between the two types, one LFSR is used as a basic counter.

An example of this is the inclusion of a many-to-LFSR counter in computerized digital values are obtained from analogue pixel counts using a timer in a CMOS image sensor. Additionally, a logically unclonable function based on a band oscillator generates a pseudo-random sequence using an array to one LFSR counter. Furthermore, a multiple phases LFSR meter was built and an array to one LFSR was integrated to run a time-of-flight camera system. The use of the LFSR for a timer has a disadvantage that must be taken into account. Given that an m-bit LFSR can have many (2m-1) states, If we want to reach 2 million states and change an LFSR state become a binary state, we will inevitably need more circuits. In addition, To avoid lowering the counting rate, the state extension needs to become synchronous with the LFSR. For example, proposed a trade-off between time and memory that combines the actions look-up table (LUT) procedure and the iteration method. Yet, when the counter size grows, the LUT size grows enormously, and the time-memory trade-off does not account for the state extension. This complicates the process of replacing an LFSR state that had binary state.

An The introduction of a multi-stage LFSR counter, whose size is exactly proportionate to the period of the decoding circuitry, occurred. and their extension dramatically slows down the counting rate. Throughout this essay, We introduce a high-speed counter linked to a new state extension. The suggested counter, which is composed of a binary and an LFSR

sub-counter, has a delay that is nearly constant for all counter sizes.

With the state detection circuit included in the proposed LFSR counter, the number of states can be increased from (2m-1) to 2m without affecting the m-bit LFSR's counting rate. Standard cells are used in the design of the test counter and the earlier counters, which are assessed in Verilog. The counting pace of the prototype counter is higher than that of the earlier counters. This is the format for the remainder of the paper. An introduction of the previous counters is provided, and then the proposed counter design with the special LFSR state extension is described. The specifics of the implementation are clarified. Lastly, a few closing thoughts are shared.

Due to their widespread usage The design of a low-power straight feedback shift registers (LFSRs) has become more important in data reduction, encryption, built-in self-testing (BIST), exchanges, and error correction circuits. In the worst situation, an LFSR's dynamic power dissipation may increase because the flip-flops' outputs may fluctuate with each clock cycle. Numerous low-power linear frequency switches have been suggested in scholarly works. An LFSR that can be reconfigured to implement any of the 16 LFSRs with representative polynomial degrees ranging from 8 to 128 is described. One of sixteen possible LFSRs can be implemented by the circuit's 128 flip-flops. A portion of all 128 flip-flops and a few XOR gates was connected to one another to create the necessary LFSR circuit in order to implement an LFSR. In this case, power dissipation is reduced by stopping the timers using the flip-flops and are not in use. Nonetheless, the LFSR functions similarly to a serial LFSR after it is set up for a specific polynomial. The low-power LFSRs use two LFSRs, each controlled by a distinct clock frequency, and are intended for BIST applications.

1.1 Low-power LFSRs

The Presented are low-power LFSRs that cut down on the number of flip-flops that change their output throughout a clock cycle. In this investigation, we have extended this technique to create an LFSR that, while retaining the characteristic A parallel LFSR in one run or the result of multiple cycles when a minimal number of flip-flops are used to modify the outputs per cycle. When numerous outputs are obtained during a single clock cycle, the clock frequency can be decreased, leading to a decrease in the voltage of the power supply. It is possible to significantly reduce power usage by modifying the LFSRs using our concept.

Replanting of the LFSR is utilised to obtain specific deterministic testing in low-power mixed-modal BIST, which also uses conventional LFSRs in serial mode. In this instance, our LFSR can be used for the identical goal of further reducing power lost. An additional method of producing test inputs that lessens transient energy presents itself at the circuit-under-test (CUT). As an example, test patterns that fall between those produced by LFSRs called intermediate test patterns. In this instance, our approach might be applied once more to significantly minimise power dissipation.

Type I and Type II LFSRs are the two varieties that are available. These two kinds of LFSRs have distinct polynomials of their own. Otherwise, if the connection is present. The Type-I LFSR's traditional serial architecture with characteristic polynomial. This instance uses two phrases that have been XORed (portrayed by) and five flip-flops as the time in LFSR. It is possible to generate signatures using BIST using any Type-I and Type-II LFSRs. But in the case of polynomial division (which is employed in the deciphering of cyclic codes), In contrast to Type-I, Type-II LFSR delivers both the proper remainder and the correct quotient. This paper's technique can be applied to Type-II LFSRs as well, making it suitable for designing decoders on cyclic codes.

Due to the fact that each clock cycle only generates one bit for data and all flip-flops are monitored in the serial design, power consumption is significant. Any flip-flop's input or output can be used to determine the output. An LFSR is a -results (or many output) LFSR where the output of subsequent cycles occurs in a single cycle. The taps are the bit locations that influence the subsequent state. The tap locations in the diagram are [16,14,13,11]. The output bit is the bit farthest to the right in the LFSR. After repeatedly XORing the taps and the output bit, the taps are sent back into the bit on the left. The output stream is the set of bits that are located in the rightmost location.

Taps are the bits that affect the input in the LFSR state. When a maximum-length LFSR is used, the shift register cycles through all conceivable states ($2m - 1$), with the exception of the state were all bits are zero. If the shift register contains all zeros, however, it will never change and instead produce an m-sequence.

In an LFSR, XNOR feedback is an alternative to XOR feedback. Although this function yields an analogous polynomial counter, which is the equivalent of an LFSR's state, it is actually an affinity map rather than a strictly linear map. Employing an A situation with all ones is illegal while utilising XNOR feedback, and a world of all zeroes is illegal when using XOR feedback. Because the till would still be "locked-up,"

this state is regarded as illegal. Since this approach is not initiated in a lockup state, it can be useful in hardware LFSRs that use flip-flops starting in a zero state. indicating that once the register is operational, it does not require seeding.

Grey code or normal binary code are two examples of binary numeral systems that are equally legitimate as the series of values generated by an XNOR equivalent or an LFSR. You can use a polynomial mod 2 in finite field arithmetic. to represent the tap configuration for response in an LFSR. This indicates that there can only be one or zero coefficients in the polynomial. This is known as the reciprocal characteristic polynomial or feedback polynomial. For instance, the feedback polynomial is where The indicated bits are where the taps are located: the 16th, 14th, 13th, and 11th.

The value fed to the primary bit (x0, which is equal to 1) is what the "one" inside the polynomial refers to, not a tapI.e. The phrases' authorities indicate the tapped bits while counting left. The first bit and the last bit are always connected as the input taps & an output tap, respectively. For every Galois field GF(2), if and only if the corresponding feedback polynomial is primitive, the LFSR has maximal-length. Accordingly, it can be said that the following prerequisites are required but not sufficient:

- There are an equal number of taps.
- The tap set is setwise co-prime, meaning that every tap must have a common divisor of 1 or greater.

The following and the references contain tables the primitive polynomials that can be used to construct maximum-length LFSRs. Multiple maximum-length tap sequences can exist for a given LFSR length. Additionally, a fixed-length tap sequence that starts at one point immediately ends at another. When an n-bit LFSR has the tap sequence The corresponding "mirror" succession is [n, n − C, n − B, n − A, 0], where the 0 indicates the x0 = 1 term. Thus, [32, 31, 30, 10, 0] is the counterpart of the tap sequence [32, 22, 2, 1, 0]. Each produces a sequence of maximum length.

2. LITERATURE REVIEW

The literature surrounding high-speed counter designs highlights the ongoing challenges and innovations in the field of digital electronics. Traditional counter architectures, particularly those based on Linear Feedback Shift Registers (LFSRs), have been limited in their state coverage, typically providing (2^m -1) states for an m-bit configuration. This limitation has prompted researchers to explore various methods to enhance the performance and efficiency of these counters. The proposed architecture in this paper addresses this gap by introducing a novel LFSR state extension technique that allows for the coverage of 2^m states without degrading the counting rate, which is a significant advancement in counter design.

Previous studies have often focused on either speed or power efficiency, but the proposed architecture successfully integrates both aspects. By employing a dual-sub-counter approach, the design optimizes the counting rate while minimizing hardware complexity. The novel LFSR counter is employed by the low-order sub-counter, and for high-order sub-counter is based on conventional synchronous binary counters. This combination not only improves performance but also addresses the challenges posed by significant fan-out in the sub-counters of high order, a common issue noted in earlier research.

Moreover, the implementation of the proposed counter in standard cells demonstrates its practical applicability, achieving a frequency of 2.08 GHz in CMOS technology using 65 nm. This performance indicates that the The counter size has little bearing on the counting rate. making the architecture highly scalable and suitable for various high-speed applications. The findings presented in this paper contribute significantly to the existing body of knowledge, offering a robust solution for high-speed counting needs in modern electronic systems, and paving the way for future research in efficient counter designs.

3. EXISTING METHOD

3.1 Previous Counters

The pre-scaled counter, LFSR, and traditional binary counter are all covered in this section. After that, a quick overview of earlier LFSR counter work is given.

3.1.1 Binary Counter

The binary sequence produced by a traditional synchronous binary counter is seen in Figure 3.1. An array of T F/Fs and a series of AND gates make up the counter. Combining an XOR gate with a D F/F can create a T F/F, as Figure 3.1's left side illustrates.

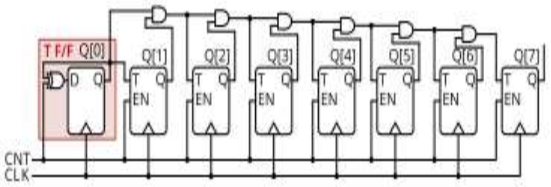


Figure 3.1 Conventional 8-bit synchronous binary counter

The CNT signal is relating to the dual EN port of both F/Fs and the XOR gate of the very initial F/F since the counter must be synchronised to both the count (CNT) signal and CLK. Because of the intrinsic features of the binary sequence, switching an upper bit is only possible

when any bottom bit is a 1. This is done by utilising a ripple carry chain, which is essentially a chain of AND gates. Given that the chain's outputs are legitimate when all of as the lesser outputs stabilize, a critical route that limits the counting rate is formed. Furthermore, the chain is not appropriate for applications requiring big counters because its propagation delay is proportionate to the counter size.

3.2 Pre-Scaled Counter

In order to obtain a An N-bit pre-scaled table, as seen in Fig. 2, was described in [19]; it provided a consistent counting rate independent of the counter size. The counter is split into two sub-counters: a high-order (N-m) low-order (m-bit) and a bit sub-counter bit sub-counter, in cases where m is significantly less than N.The high-order sub-counter can function with a lengthy clock period because the ith bit of the numbering results is swapped every 2i clock cycles [7], [20].Even in cases where the low-order sub-counter's size is less than or equal to six bits, the slow clock is adequate for the high-order sub-counter [19].In Fig. 2, the upper right corner, A straight ring counter can have simply its leftmost F/F initialised to 1, or it can have the opposing ring rotated right by one clock cycle. This is done to enable the high-order sub-counter once the low-order sub-counter is counted 2m states. Two significant issues need to be solved with the pre-scaled counters: first, the number of F/Fs needed grows exponentially with m, because the straight ring counter's size is proportional to 2m. It usually takes more F/Fs to build a traditional ring counter (2m) than it does to build a baseline counter. even if the dimension m on the low-order sub-counter isn't very largen. Due to the second reason—that is, the pre-scaled count is not operating at the anticipated speed—a substantial fan-out is required when (N-m) bits are driven by the pre-scaler enabled (PEN) signal.

3.3 Linear Feedback Shift Register (LFSR)

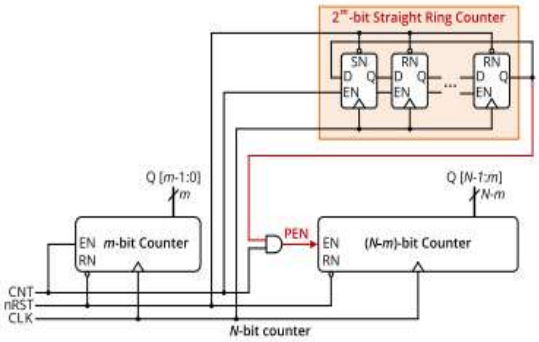


Figure 3.2 N-bit pre-scaled counter

Traditional LFSR: A linear feedback network represents the input-to-output relationship in an LFSR, which is a type of shift register. Generally, a linear connection is represented as a digital polynomial to show where the taps that influence the subsequent state are located. Additionally, XOR gates are used to implement the relationship, which enables the LFSR to produce a series of pseudo-random integers. Two different 8-bit LFSR types are depicted in Figure 3.2: Figure 3.2a depicts a many-to-one type, while Figure 3.2b depicts a one-to-many type. There is a common term for both of them: Fibonacci LFSR and Galois LFSR. Both of the 8-bit Four-, five-, six-, and eight-bit taps are present in LFSRs. Polynomial x8 ÷ x6 á x5 á x4 á 1; (1) can be used to represent them, with the last 1 corresponding to x0 denoting the input to Q [0]. It is possible to configure the initial value into the LFSR by choosing

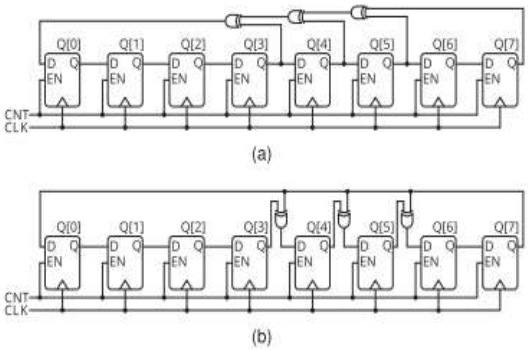


Figure 3.3 LFSR types (a) Many-to-one LFSR and (b) one-to-many LFSR with 4taps

F/Fs having the ability to set and reset. Two counters operate at different rates, although sharing similarities with regard to the total amount of taps and the corresponding polynomial. XORing the signals originating from the taps yields the feedback signal in the case of many-to-one LFSR. As more taps are made, the feedback signal slows down. On the other hand, with its one-to-many LFSR, Fig. 3b's final F/F Q [7] determines every tap. indicating that in terms of operation speed, the one-to-many LFSR is faster than the many-to-one LFSR.A set of taps that corresponds to longest sequence is needed in order to employ an LFSR as a counter. Primitive polynomials are combinations of taps that have the maximum-length sequence; they have a length of (2m -1) states, with the exception of the state where all bits are 0. One state needs to be extended in order to create a sequence of two million states, as the maximum length is a member less than two million.

3.3.1 Multistage LFSR Counter

The multiple phases LFSR count produces similar m-bit LFSR blocks and concatenate to create a 2m-state count, as shown in Figure 3.2. Combining the feedback and state extension into a single block reduces the overall hardware complexity of the redesigned circuit,

as shown in Fig. 4a. It inserts the missing state by turning off the feedback path upon detecting a LFSR state Q[m1:0] of 100...02. Still, the (m-1)-input A sequence of tiny NOR gates is what is used to detect the LFSR state. OR and NOR gates, As a result, the state detection delay and the AND-gate chain are comparable. delay of a traditional binary counter. As anticipated, the m-bit LFSR s not as fast because The block counter size affects the state detection delay. For the LFSR blocks [12], whose lengths vary from 3 bits to 10 bits, Table 1 displays their critical path. For all block sizes, the combination of feedback and state expansion induces a critical route. As the size of every LFSR block [12] rises, the level of criticality tends to increase.

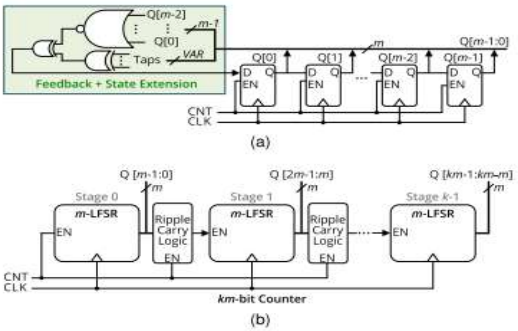


Figure 3.4 Multistage LFSR counter. (a) An m-bit LFSR block with state extension, and (b) the overall block diagram.

To maintain small values of m and ultimately decrease the total number of LUT entries needed to perform state conversion down 2m to 2km, every multiple phases LFSR counter is separated into k m-LFSR, as seen in Fig. 4b. Between successive stages, rippled carry logic that enables the addition of the subsequent LFSR block because traversing 2km states requires ruling the km-bit counter.. The next step is switched once to the rippled carry logic upon detecting an LFSR state that is 11...102. However, a ripple fault that changes all succeeding stages and the next stage consecutively can be caused by the structure. Stated differently, the ripple error must be rectified by adding a new circuit.

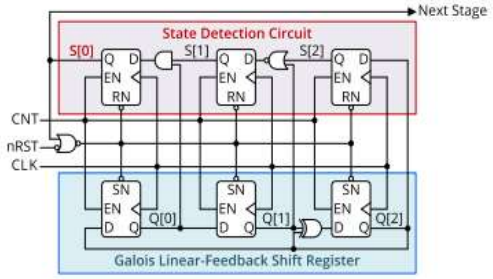
4. PROPOSED METHOD

4.1 Proposed High-Speed Counter

This section first discusses the proposed LFSR counters with new state detection, then goes into great length into the general design of the high-speed counter. 3.1 LFSR Counter Proposed with State Extension Figure 4.1a illustrates a proposed LFSR counter after state extension, whereas Figures 4.2b and 4.3c show a set of LFSR states free of and with the extension, respectively. An example of the concept is provided by using a 3-bit LFSR counter using two taps, Q[1] and Q[2], since the suggested method can be applied to any size of LFSR. As Fig. 5a illustrates, the suggested LFSR consists of a state sensing circuit and a Galois LFSR. The CNT signal activates the counter, which is synchronised with time and reset (nRST) signal. The state detecting circuit is initialised to 0002 and then Galois LFSR is initialised to 1112 either nRST is 0 or S [0] is 1. States 1112 through 1012 are produced using the traditional 3-bit LFSR in Fig. 5b, however state 0002 is not included in this sequence.

Table 1 Critical Path of the LFSR blocks [12] With State Extension

LFSR Block Size (bits)	Critical Path
3	Q → XOR2→XOR2→D*
4	Q → XOR2→XOR2→D
5	Q → NOR4→XOR2→D
6	Q → OR2→NOR3→XOR2→D
7	Q → OR2→NOR3→XOR2→D
8	Q → OR2→NOR4→XOR2→D
9	Q → OR2→NOR4→XOR2→D
10	Q → OR3→NOR3→XOR2→D



State	Q[2]	Q[1]	Q[0]
0	1	1	1
1	0	1	1
2	1	1	0
3	0	0	1
4	0	1	0
5	1	0	0
6	1	0	1

(b)

State	Q[2]	Q[1]	Q[0]	S[2]	S[1]	S[0]
0	1	1	1	0	0	0
1	0	1	1	1	0	0
2	1	1	0	0	0	0
3	0	0	1	1	0	0
4	0	1	0	0	0	0
5	1	0	0	0	0	0
6	1	0	1	1	1	0
7	1	1	1	1	0	1

RESET

(c)

Figure 4.1 (a) The proposed 3-bit LFSR counter with the proposed state detection cir- cuit, (b) states of the conventional 3-bit LFSR counter with a primitive polynomial x3 + x2 +1, and (c) states of the LFSR counter with the proposed state extension.

To increase the number of phases to 2m, we require a unique technique because an m-bit LFSR can only produce (2m-1).By taking three consecutive cycles into consideration, the state recognition circuit in Figure 4.1a finds an arc bit-pattern of 0012, that is indicated with a solid circle as Figure 4.1b. The initial motif 02 of the diagonally pattern is recognized by its final F/F S[2] in the situation detection circuit. Next, It of 002 on the next cycle is identified by F/F S[1] using the 02 pattern discovered in S[2]. Finally, based on the 002 pattern that S [1] observed, the initial F/F S[0] identifies the 0012 pattern during the following cycle. These detections are shown as dotted lines in Figure 4.1c. Upon detecting the vertical pattern of 0012, S [0] turns into 1, which subsequently resets the situation detection circuit and the LFSR during the subsequent cycle. resulting in two states of Q [2:0] = 1112 in succession. Still, by looking at the number of S [0], stages 0 and 7 can be distinguished from one another.

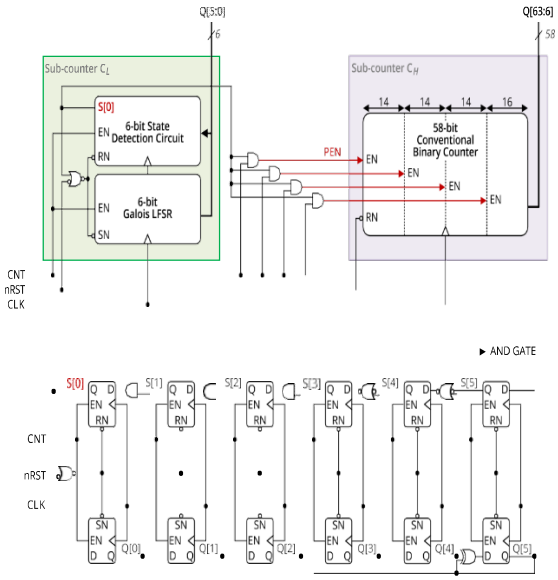
An m-bit LFSR can be implemented using this approach. and by permuting the bit order and choosing a suitable initial value, It is possible to reset the LFSR by using a unique diagonal pattern that we have discovered. S [m-1] is instantly hooked to Q [m-1]. given a trend of m bits; at all other positions, S[i] is latched into Q[i] based on the value calculated from Q[i] and S[i + 1]. To find the diagonal pattern, this method is done m times. A few possible Low-order micro counter variants of the proposed LFSR counter can be implemented. are displayed in Table 2. Every LFSR counter that was tested had a distinct detecting pattern, and additional detecting patterns may be discovered while examining several primitive polynomials. As is usually the case when an uncommon lateral pattern is gradually identified bit by bit, the recommended situation detect circuit's delay is mostly composed of a gate delay plus some additional delay components needed to access F/Fs.

similar to the interval in the feedback path of an LFSR with an XOR gate. When employed in a state detection circuit, an XOR gate often has a greater delay than a basic gate. Consequently, there is a rate of

The suggested LFSR counter resembles the traditional Galois LFSR in many ways. Table 3 displays the single-stage LFSR block counters' vital route. Obviously, the feedback connection offers the most important path for all LFSR sizes.

4.2 Implementation Details

This section presents a comparison the traditional synchronous binary counter and the multistage LFSR counter [12]. The performance is examined in relation to the highest rate of counting The hardware complexity and maximum counting rate of reasonably sized counters with a bit range of 16 to 64, as well as single-stage block counters with a bit range of 3 to 10 bits. Every counter uses standard cells made with 65 nm CMOS chips. The temperature is 25 ◦C and the operational voltage is 1.2 V while measuring the counting rate. As seen in Fig. 4b, the multiple stages LFSR counter [12] is constructed by serially concatenating 8-bit LFSRs, in contrast to the typical binary counter, which is realized in a single stage. The recommended clock in Fig. 7a couples a 6-bit LFSR constant with a 58-bit digital counter to form a 64-bit counter.. The sixth-order polynomial in Table 2 serves as the foundation for the 6-bit LFSR counter depicted in Fig. 7b, where ⅂[5] is connected to S[0] rather than S[5]. In Figure 7c, a solid circle indicates that the recommended state detecting circuit detects a specific diagonal pattern of 1001112. Remember this.



State	Q[4]	Q[3]	Q[2]	Q[1]	Q[0]	Q[5]	S[5]	S[4]	S[3]	S[2]	S[1]	S[0]
0	1	1	1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	0	1	0	0	0	0	0
2	1	1	1	1	0	1	1	0	0	0	0	0

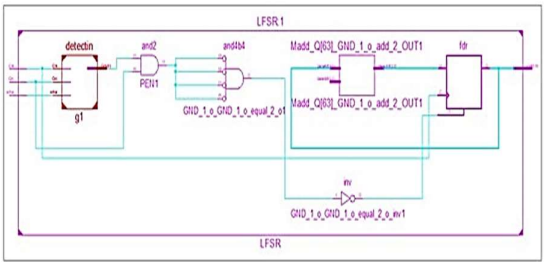
56	0	1	0	0	0	0	0	0	0	0	0	0
57	1	0	0	0	0	0	0	0	0	0	0	0
58	0	0	0	0	0	1	0	0	0	0	0	0
59	0	0	0	0	1	1	0	1	0	0	0	0
60	0	0	0	1	1	1	0	0	1	0	0	0
61	0	0	1	1	1	1	0	0	0	1	0	0
62	0	1	1	1	1	1	0	0	0	0	1	0
63	1	1	1	1	1	1	0	0	0	0	0	1

Figure 4.2 The proposed 64-bit counter. (a) The overall structure, (b) the 6-bit LFSR counter with the proposed state detection, and (c) its state changes.

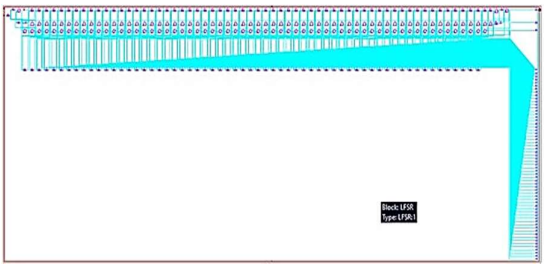
The purpose of the binary counter in Figure 4.2a is to minimise the delay resulting from the big fan-out by utilising PEN signals. The four AND gates in the suggested counter drive 14, 14, 14, and 16 F/Fs apiece. By simply decreasing the binary counter's size, the 64-bit structure can likewise be utilised to create smaller counters. It implies that many smaller-sized counters can be commonly realised using the 6-bit LFSR counter. Drive gates can be lowered in accordance with a decrease in the binary counter's size.

5. RESULTS

RTL schematic:



Technology Schematic:



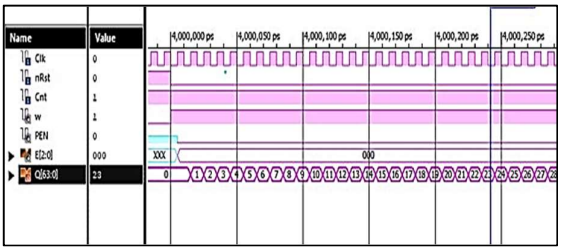
Delay:

```
Delay:               2.914ns (Levels of Logic = 65)
  Source:            Q_0 (FF)
  Destination:       Q_63 (FF)
  Source Clock:      Clk rising
  Destination Clock: Clk rising

  Data Path: Q_0 to Q_63
```

Area:

```
Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:             64  out of  126800     0%
 Number of Slice LUTs:                  64  out of  63400      0%
    Number used as Logic:               64  out of  63400      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    64
   Number with an unused Flip Flop:      0  out of     64     0%
   Number with an unused LUT:            0  out of     64     0%
   Number of fully used LUT-FF pairs:   64  out of     64   100%
   Number of unique control sets:        1

IO Utilization:
 Number of IOs:                         67
 Number of bonded IOBs:                 65  out of    210    30%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:              1  out of     32     3%
```

Simulation:



CONCLUSION

In order to limit the latency that arises from identifying the LFSR state of a cycle, just one bit is considered. It results in an angled m-bit pattern detectable for m cycles. Using (m-1) gates and m F/Fs, this distinct diagonal pattern is found. Using a prescaled basic counter and setting it to the top bit positions is how the proposed counter—which is founded on a small LFSR counter—is implemented. The proposed 64-bit counter, in other words, is composed of two sub-counters: a 6-bit LFSR account at the lower bit positions & a conventional 58-bit binary clock at the greater bit positions. By detecting a certain state, the suggested A conventional pre-scaled counter requires a straight ring count to ensure that the two sub-counters count appropriately, while an LFSR counter only permits the numbering of one high-order sub-counter. The suggested m-bit LFSR counter traverses 2m states as quickly as the traditional LFSR thanks to the innovative state extension technique. so the suggested counter's counting pace is mostly unaffected by the counter's size.

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