Design And Comparative Analysis of Two Stage CMOS Operational Amplifier under Technology Scaling (180nm to 90nm)

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***Abstract* — As we move from smaller and faster devices in VLSI Industry, circuit designers are facing problems maintaining the performance and higher speed of operation of circuits. This paper explores the design comparison of two stage operational amplifiers in 180nm and 90nm technology nodes. By keeping supply voltage (V_{DD}) at 1.8 V and load capacitor value as C_L=1pF, we were able to understand the effect of scaling in performance of two stage operational amplifier circuit.**

Our findings from this study is that scaling down from 180nm to 90nm provided greater speed at the cost of DC gain. Gain Bandwidth product has been moved from 20.1 MHz to 24 MHz, whereas Gain has decreased from 63.50 dB to 55.22 dB. This drop in gain is a direct consequence of the reduction of output resistance in shorter channel length (90nm). Despite the shift in gain, both designs are remarkably stable as phase margin is in the range of (72°-75°). By providing a side-by-side quantitative breakdown of gain, bandwidth and slew rate, this study plays an important role for designers to understand the benefits and drawbacks of scaling down in Analog VLSI design.

Keywords - Op-Amp, Technology Scaling, 180 nm, 90 nm, Analog VLSI Design, Gain-Bandwidth Trade-off, Short-Channel Effects.

I. Introduction

The continuous advancement of Very Large-Scale Integration (VLSI) technology has significantly transformed the semiconductor industry, enabling higher integration density, faster operation, and reduced power consumption in digital circuits [7], [8]. As technology scales from micrometer to deep submicron regimes such as 180 nm and 90 nm, the benefits for digital systems are substantial. However, this aggressive scaling introduces critical challenges for analog circuit design, particularly for fundamental building blocks like operational amplifiers (Op-Amps) [1], [2].

Operational amplifiers play a crucial role in a wide range of analog and mixed-signal applications, including analog-to-digital converters (ADCs), digital-to-analog converters (DACs), active filters, voltage regulators, and sensor interface circuits [6]. The performance of these systems heavily depends on the accuracy, stability, and speed of the op-amp. Traditionally, larger technology nodes such as 180 nm allow designers to achieve high gain and better linearity due to higher output resistance and larger device dimensions [4], [5].

However, as the technology scales down to 90 nm, several non-ideal effects become more prominent. Short-channel effects reduce intrinsic gain, increase leakage currents, and limit voltage headroom [1], [3]. Additionally, lower supply voltages restrict signal swing and complicate biasing conditions, making it difficult to maintain high gain and stability simultaneously [2], [10].

These limitations demand careful design strategies, including proper device sizing, biasing techniques, and compensation methods. Among various op-amp architectures, the two-stage CMOS op-amp with Miller compensation remains widely used due to its ability to provide high gain and sufficient output swing while maintaining stability [3], [9].

This work focuses on designing an amplifier and analyzing its performance under two different technology nodes—180 nm and 90 nm. By maintaining identical operating conditions, this study aims to clearly highlight the impact of technology scaling on key performance parameters and provide a deeper understanding of the associated trade-offs.

II. Literature Survey

The design and optimization of CMOS operational amplifiers have been extensively studied in the field of analog VLSI design, particularly in the context of technology scaling [7], [8]. As CMOS technology has evolved from long-channel to short-channel devices, researchers have observed significant changes in analog circuit behavior, especially in parameters such as gain, bandwidth, power consumption, and noise performance [6].

Several studies have focused on the design of two-stage CMOS operational amplifiers in 180 nm technology, emphasizing high gain, low power consumption, and improved common-mode rejection ratio (CMRR) [4], [5], [9]. These works highlight that larger channel lengths contribute to higher output resistance, which directly enhances voltage gain and overall amplifier performance. Additionally, the availability of higher supply voltages in 180 nm technology provides better signal swing and simplifies biasing conditions.

On the other hand, research on 90 nm technology demonstrates improved speed and reduced power consumption due to lower parasitic capacitances and higher transconductance [1], [2]. However, these advantages come with significant challenges. Authors have reported a noticeable reduction in intrinsic gain

caused by decreased output resistance and stronger short-channel effects [3]. Furthermore, reduced supply voltages limit the dynamic range and complicate circuit design.

To address stability issues in scaled technologies, compensation techniques such as Miller compensation have been widely adopted [3], [10]. Literature indicates that proper selection of compensation capacitors and bias currents is essential to achieve an adequate phase margin and prevent oscillations. Advanced techniques such as gain boosting and cascode configurations have also been explored to enhance gain in deep submicron technologies [6].

Despite extensive research, there remains a need for a direct and fair comparison of op-amp performance across different technology nodes under identical conditions. Most existing works focus on a single technology or vary operating parameters, making it difficult to quantify the exact impact of scaling. This study bridges that gap by presenting a side-by-side comparative analysis of 180 nm and 90 nm CMOS op-amps using standardized specifications, thereby providing clear insights into the trade-offs between gain, speed, and power efficiency in modern analog design.

III. METHODOLOGY

Initially, the desired specifications were decided for both 90nm and 180nm. Parameters like Gain, unity gain bandwidth, slew rate, Phase margin were targeted same for both technologies. The circuit was made using a two stage CMOS amplifier topology in which the first stage is Differential Amplifier stage followed by a Common Source amplifier stage which is the high gain stage. Current mirror is used as biasing circuit to get stable bias currents. A Miller compensated capacitor (Cc) is used between these stages to ensure stability. The aspect ratio for sizing each transistor is calculated using the design equations to meet the targets. The channel length was kept 500n for both 180nm and 90nm and widths were calculated according to get the transconductance. The current mirrors were also sized in a way to get proper biasing currents. The simulations were carried out using EDA tool Cadence Virtuoso. We started by finding the values of βeff to calculate the transconductance parameters. Next AC analysis was done to get gain and phase margin plot. DC analysis was done to calculate the values of gain and was matched it with the plotted values. AC analysis and DC analysis were carried out for both ICMR(+) as well as ICMR(-). For slew rate, transient analysis was done by using step input. Device dimensions and biasing currents were adjusted if performance was not satisfactory. The simulations were carried out under same conditions for both technologies. Finally, the comparison was made based on Gain, Phase margin, Bandwidth and slew rate. By observing the effect of scaling on these parameters helped us understand the tradeoffs between these technologies.

TABLE I

Decided parameters and specifications

Parameters	Specifications
DC Gain	>= 60 dB
GBW	25 MHz
Phase Margin	>= 60°
Slew rate	25 V/µs
ICMR(+)	1.6 V
ICMR(-)	0.8 V
C_L	1pF
VDD	1.8 V
Power Dissipation (PD)	<= 400 uW

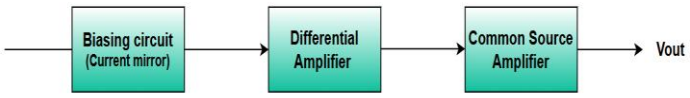

Fig. 1. Block diagram of Two Stage Op-amp.

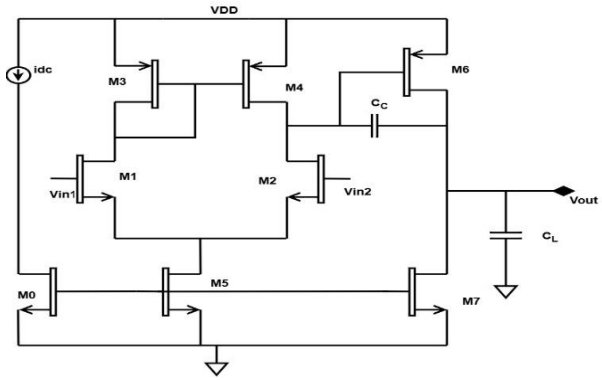

Fig. 2. Circuit diagram of Two Stage Op-amp.

CALCULATIONS

Calculation of $\mu ncox$ and $\mu pcox$:

$$\mu ncox = \frac{\beta eff}{\left(\frac{W}{L}\right)} = \frac{Beff \times L}{W}$$

$$\mu pcox = \frac{\beta eff}{\left(\frac{W}{L}\right)} = \frac{Beff \times L}{W}$$

TABLE II

Values of uncox and upcox for 180 nm and 90 nm technologies

Technology	$\mu ncox$	$\mu pcox$
180 nm	$300\mu A/V^2$	$60\mu A/V^2$
90 nm	$316\mu A/V^2$	$142\mu A/V^2$

Calculation of C_c:

$$C_c \geq 0.22 \times C_L$$

Calculation of I_5:

$$Slew\ Rate(SR) = \frac{I_5}{C_c}$$

$$I_5 = SR \times C_c$$

Design of M_1, M_2:

$$gm_1 = GB \times C_c \times 2\pi$$

$$gm^2 = 2I_D\ \mu ncox \left(\frac{w}{l}\right)$$

$$\left(\frac{w}{l}\right)_1 = \frac{gm^2}{\mu ncox\ .\ 2I_D} = \frac{gm^2}{\mu ncox\ .\ I_5}$$

Finding the value of Vth_{max} and Vth_{min} for PMOS and NMOS:

TABLE III

Comparison table of parameters of 180nm and 90nm technologies

Technology	180 nm	90 nm
$V_{th1\ min}$ (mV)	536.162	249.767
$V_{th1\ max}$ (mV)	677.56	331.539
$V_{th3\ min}$(mV)	-473.288	-186.479
$V_{th3\ max}$ (mV)	-458.373	-186.479

Calculating the $\left(\frac{w}{l}\right)$ $ratio\ for\ M_3\ and\ M_4$:

M_3 $will\ be\ in\ saturation$

$V_g < V_{D1} + V_{th1}$

$V_{in} < V_{D1} + V_{th1}$

$V_{in\ max} < V_{D1} + V_{th1}$ ..... (1)

$V_{D1} < V_{DD} - V_{sg3}$

$$I_3 = \frac{\mu ncox \left(\frac{w}{l}\right)}{2} \left(V_{gs} - V_{th}\right)^2$$

$$V_{gs} = \sqrt{\frac{2I_3}{\beta}} + |V_{th3}|$$

$$V_{D1} < V_{DD} - \left(\sqrt{\frac{2I_3}{\beta}} + |V_{th3}|\right)$$

From equation (1)

$$V_{in\ max} < \underbrace{V_{D1} + V_{th1}}_{\min}$$

ICMR + $\leq V_{D1\ min} - V_{th1\ min}$

$V_{in\ max} \leq V_{D1min} + V_{th1min}$

$$ICMR+ \leq V_{DD} - \sqrt{\frac{2I_{D3}}{\beta_3}} - |V_{th3\ min}| + V_{th1\ min}$$

$$\left(\frac{w}{l}\right)_3 = \frac{2I_{D3}}{\mu pcox\ .\ [V_{DD} - ICMR(+) - V_{th3\ max} + V_{th1\ min}]}$$

Calculating the $\left(\frac{w}{l}\right)$ $ratio\ for\ M_5$:

Transistor M_5 is mirror of M_0

For M_5 $to\ be\ saturation$

$$V_{D\ sat} \geq ICMR(-) - \sqrt{\frac{2I_{D1}}{\beta_3}} - V_{th1\ max}$$

$$I_{D5} = \frac{\mu pcox \left(\frac{w}{l}\right) (V_{D\ sat})^2}{2}$$

$$\left(\frac{w}{l}\right)_5 = \frac{2I_{D5}}{\mu ncox\ .\ (V_{D\ sat})^2}$$

Calculating the $\left(\frac{w}{l}\right)$ $ratio\ for\ M_6$:

For 60° $phase\ margin$

$gm_6 \geq 10\ .\ gm_6$

$$\frac{\left(\frac{w}{l}\right)_6}{\left(\frac{w}{l}\right)_4} = \frac{I_6}{I_4} = \frac{gm_6}{gm_4}$$

$$\left(\frac{w}{l}\right)_6 = \frac{gm_6}{gm_4} . \left(\frac{w}{l}\right)_4$$

Calculating the $\left(\frac{w}{l}\right)$ $ratio\ for\ M_7$:

Transistor M_7 is mirror of M_0

$$\frac{I_6}{I_4} = \frac{\left(\frac{w}{l}\right)_6}{\left(\frac{w}{l}\right)_4}$$

$$\frac{I_7}{I_5} = \frac{\left(\frac{W}{l}\right)_7}{\left(\frac{W}{l}\right)_5}$$

$$\left(\frac{W}{l}\right)_7 = \frac{I_7}{I_5} \cdot \left(\frac{W}{l}\right)_5$$

TABLE IV

Aspect ratio for 180nm and 90nm technology

L = 500nm for all the transistors

Technology	180 nm	90 nm
MOSFET	Wn (um)	Wn (um)
M0	W0 = 1	W0 = 0.53
M1	W1 = 1	W1 = 2
M2	W2 = 1	W2 = 2
M3	W3 = 3	W3 = 1
M4	W4 = 3	W4 = 1
M5	W5 = 14	W5 = 0.53
M6	W6 = 38	W6 = 18
M7	W7 = 90	W7 = 5.535

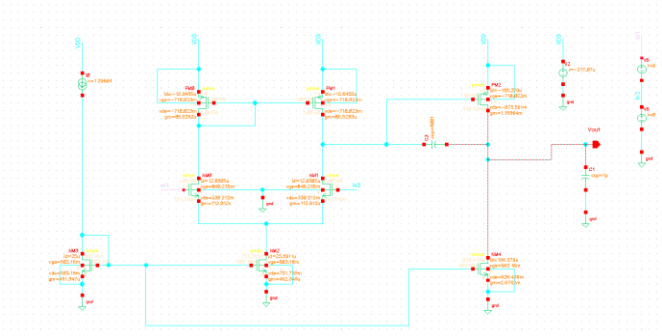

Fig. 3. Simulation circuit of 180 nm.

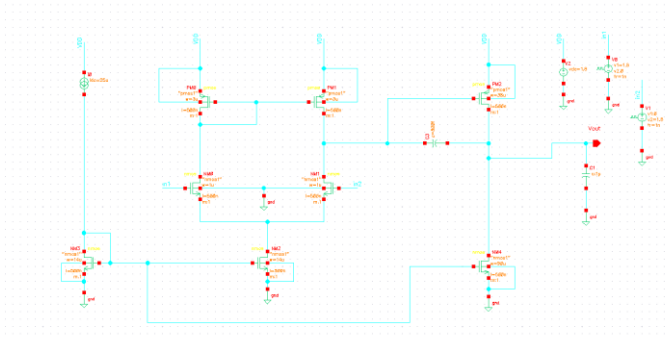

Fig. 4. Slew rate circuit of 180 nm.

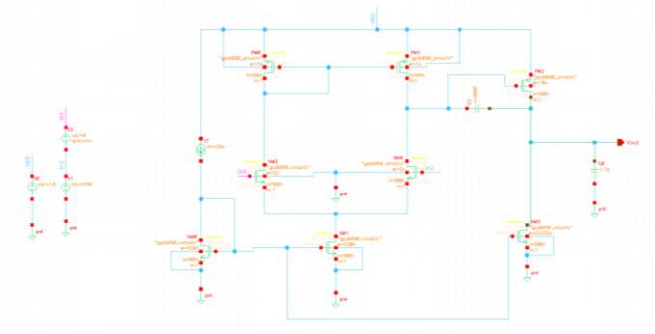

Fig. 5. Simulation circuit of 90 nm.

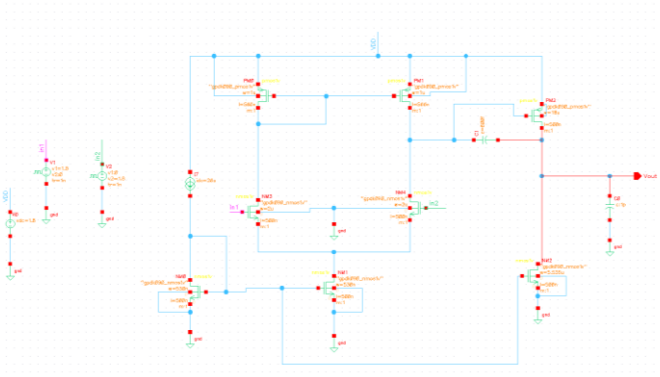

Fig. 6. Slew rate circuit of 90 nm.

IV. RESULTS

The CMOS two-stage op-amp was designed and simulated in both 180 nm and 90 nm technologies using Cadence Virtuoso with the Spectre simulator. The design was carried out by keeping the supply voltage fixed at 1.8 V and load capacitance at 1 pF for both technology nodes to ensure a fair comparison. Efforts were made to optimize key performance parameters such as DC gain, phase margin, gain-bandwidth product (GBW), and slew rate. From the simulation results, the 180 nm op-amp exhibits better DC gain, achieving a maximum value of 63.504 dB. The phase margin is around 73.24°, ensuring stable operation, while the gain-bandwidth product is approximately 20.1 MHz. The slew rate reaches up to 25.99 V/µs, making this design suitable for applications like switched capacitor filters, analog-to-digital converters, and instrumentation amplifiers. In comparison, the 90 nm op-amp shows improved dynamic performance. The gain-bandwidth product increases to around 23–24 MHz and the slew rate also improves, indicating faster response due to reduced parasitic capacitances and higher transconductance in smaller technology. However, the DC gain drops to around 53.20 dB, mainly due to short-channel effects, which reduce the output resistance of transistors. This behavior aligns with the scaling trend $A_v \propto 1/L$. The phase margin for the 90 nm design remains above 73°, similar to the 180 nm case, confirming that stability is maintained in both implementations. Overall, the results highlight a clear trade-off: the 180 nm design provides higher gain, while the 90 nm design offers better speed. Both designs are stable and meet the required specifications, making them suitable for different analog applications depending on the design priority.

TABLE V
Comparison table of parameters of 180nm and 90nm technologies

Technology	180 nm		90 nm	
Parameter	Vcm=0.8V	Vcm=1.6V	Vcm=0.8V	Vcm=1.6V
Gain (dB)	63.504	60.424	53.2026	55.226
Phase margin (°)	73.2403	73.2298	75.6403	74.788
Slew rate (V/µs)	16.107		25.299	
GBW (MHz)	20.1	20.5	23.060	23.9883

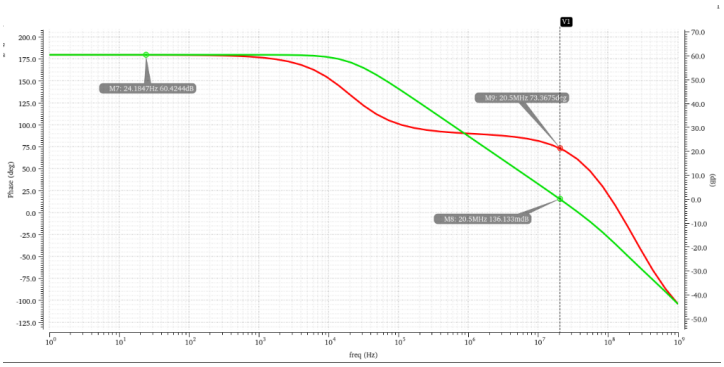

Fig. 7. Gain, Phase margin and GBW at Vcm=1.6V for 180nm technology

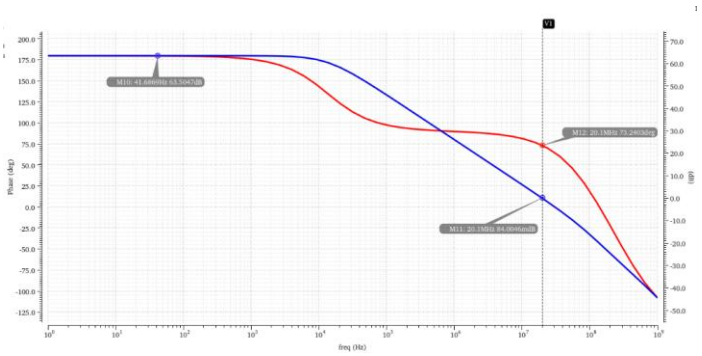

Fig. 8. Gain, Phase margin and GBW at Vcm=0.8V for 180nm technology

Fig. 9. Slew rate for 180nm technology

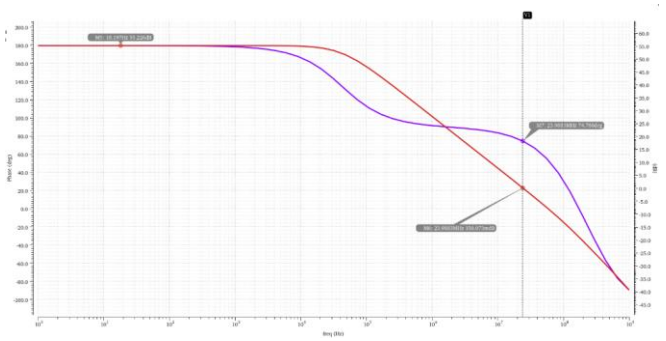

Fig. 10. Gain, Phase margin and GBW at Vcm=1.6V for 90nm technology

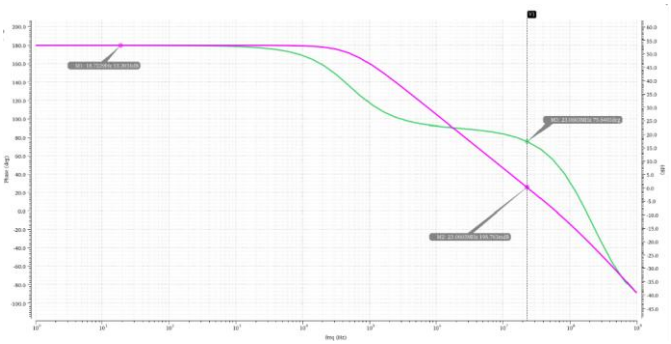

Fig. 11. Gain, Phase margin and GBW at Vcm=0.8V for 90nm technology

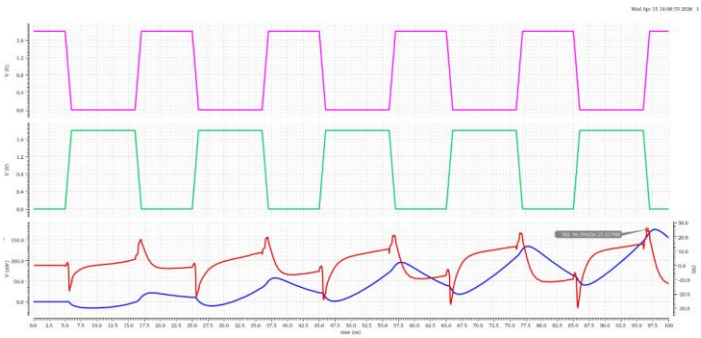

Fig. 12. Slew rate for 90nm technology

V. CONCLUSION

A two-stage CMOS operational amplifier was designed and analyzed using both 180 nm and 90 nm technologies under the same operating specifications listed in the above table I. This allowed a direct comparison of how technology scaling influences key analog performance parameters. The results shows that reducing the technology node improves the gain-bandwidth product and slew rate. The 90 nm design shows better performance and efficiency, mainly because of reduced unwanted effects and faster device speeds.

On the other hand, the DC gain shows a decline in the 90 nm implementation. This is mostly because smaller channel lengths reduces the output resistance of MOS devices, it directly affects the overall gain of the amplifiers. This limits, both designs maintain sufficient phase margin, confirming that stability has been preserved through proper compensation. The comparison clearly shows that technology scaling introduce trade-offs rather than

absolute improvements. While speed and efficiency benefit from scaling, achieving high gain becomes more difficult and requires careful design choices. Parameters such as device sizing, biasing, and compensation need more attention in smaller technologies.

In conclusion, analog design in deep submicron technologies demands a balanced and thoughtful approach. The choice between 180 nm and 90 nm depends on application requirements whether the priority is higher gain or improved speed. This study emphasizes the importance of understanding these trade-offs for effective analog circuit design.

VI. FUTURE SCOPE

The proposed design meets the performance standards, but there is still room for improvements and more research. A way to improve the design is to improve the DC gain using advanced methods like cascode configurations or gain boosting. These methods help to boost the overall gain and output resistance (r_0), without affecting bandwidth. More advanced compensation strategies can be explored in order to get a better gain bandwidth trade off while keeping stability. The proposed design can also be used with more advanced technologies like 45 nm or even smaller. By observing how amplifier will work at these small scales, we can explore more about how scaling affects parameters like noise and frequency response. Further work can be done by implementing layout level designs and then later running post layout simulations. This step is important as it takes into account parasitic capacitances and resistances, which can have a big effect on how well things work in the real world compared to that working in a schematic. The amplifier can be put into real world analog or mixed signal systems like ADCs or filters to observe how they work in real life. The design can also be further improved to observe its power consumption.

VII. REFERENCES

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