ASIC IMPLEMENTATION OF MEDIAN FILTER USING CO-DESIGN WITH CLOCK GATING TECHNIQUE

Padmini G. Kaushik[1*], Dr. S.M.Gulhane[2]

[1]Research Scholar, Department of E&TC Engineering, JDIET, Yavatmal, Maharashtra, India

[2]Professor, Pravara Rural Engineering College, Loni, Maharashtra, India.

ABSTRACT

The increasing popularity of portable devices and consumer electronics has led to the focus of VLSI on improving energy efficiency and reducing power consumption. Reduction of power is accomplished at every level of VLSI chip design, from the highest level of architecture to the most basic block design, all of which are implemented in gate level. The clock signal is significant in the dynamic power consumption equation, it can account for as much as 50% of the total power consumption. Power optimization is important for all parts of the system on chip design process, from the initial design stages to the final stages. The concept of hardware and software co-design is characterized by the combined implementation of hardware and software. The objective of co-design is to reduce the manufacturing time while simultaneously increasing the structure's expenditure and planned items. The research work aims to efficiently deploy the hardware-software co-design strategy in association with Clock gating technique in a mission-critical design environment and compare the achieved power reduction with the other counterparts without the use of hardware and software co-design strategy. The power reduction by the proposed Co-design with Clock Gating technique is an application specific and the research work achieves an overall power reduction for median filter is about 98 %.

KEYWORDS: Median Filter, ASIC, Clock gating, Hardware-Software Co-design, Power reduction

INTRODUCTION

As the demand for low-powered mobile computers and consumer electronics has increased, VLSI designs have adopted a philosophy of prioritizing low power consumption and efficiency. The attention of the world was initially dedicated to the power consumption between 1990 and 1992, during this time, only certain markets required low-power computers (1). In the past, the capacity of chips was limited by their size, but today, power is the primary obstacle. The words "high performance" and "energy efficiency" are now frequently used as synonymous terms. Earlier, scientists and designers of Very Large-Scale Integrated

Circuits (VLSI) focused on speed as the primary concern for efficiency. It's common knowledge that high performance and small space are in conflict. As a result, the primary concern of IC design has been addressing this specific issue. In 1992, the original Alpha processor had a speed of 200 MHz, which was still quite impressive for its time. However, it also had a high power consumption rate of approximately 30 watts. The main goal of any design is to effectively fulfill system requirements. This entails discovering a resolution that balances the competing requests of the system, financial feasibility, and ecological impact. Concentrating solely on one of these aspects will only fulfill a fraction of the comprehensive requirements. VLSI (Very Large Scale Integration) chip design is a field that continues to evolve rapidly, driven by the demand for more powerful and energy-efficient integrated circuits. As we move towards smaller process nodes and more complex chip designs, a number of challenges and trends have emerged, particularly in the realm of energy efficiency and power consumption reduction. One of the key trends in VLSI chip design is the continuous shrinking of process nodes. As feature sizes decrease, more transistors can be packed onto a single chip, leading to higher performance. However, smaller process nodes also bring challenges such as increased leakage currents and variability, which can impact energy efficiency. Increased Integration and Complexity: Modern VLSI chips are becoming increasingly complex, with a growing number of cores, functional units, and peripherals integrated onto a single die. This complexity poses challenges for power optimization strategies as managing power consumption becomes more difficult in highly integrated systems.

Dynamic power consumption, which is the power consumed by the switching of transistors is a significant factor in overall power consumption. As clock frequencies and data rates increase, managing dynamic power becomes crucial for energy efficiency. Static Power Consumption: Static power consumption, or leakage power, has become a major concern as process nodes shrink. Leakage currents through transistors that are supposed to be turned off can significantly impact energy efficiency, especially in idle or low-power modes. Variability and Reliability: With shrinking process nodes, variability in manufacturing processes becomes more pronounced, leading to variations in performance and power consumption among different chips. (2) Managing this variability is crucial for ensuring reliable operation and optimal power efficiency. Design for Low Power: Designing chips for low power consumption has become a primary focus in VLSI chip design. Techniques such as power gating, clock gating, voltage scaling, and dynamic voltage and frequency scaling (DVFS) are commonly used to optimize power consumption in modern integrated circuits. Advanced

Power Management: Advanced power management techniques, such as multiple power domains, power islands, and adaptive voltage scaling, are being employed to dynamically adjust power consumption based on workload requirements and operating conditions. Emerging Technologies: Emerging technologies such as 3D integration, non-volatile memories, and novel transistor structures offer new opportunities for improving energy efficiency in VLSI chip design. These technologies enable designers to explore new power optimization strategies and design methodologies (3).

Co-designing hardware (HW) and software (SW) involves not only the combination of two separate design strategies, but also the integration of HW and SW components (4). The design process also requires a balance between the system's flexibility and performance. The main challenge in HW/ SW co-design is to achieve a balance between parallel and sequential implementation. The effectiveness of the HW/ SW co-design is highly dependent on the selection of the appropriate HW/ SW design methodology. Co-designing hardware and software refers to the unification of both elements into a unified implementation (5).

The primary objective of the research is to minimize the amount of power consumed by digital circuits. Through the utilization of the Co-design method, combined with technology that regulates the clock frequency. The practice of co-design allows for necessary flexibility in order to reduce power significantly.

The contrast between proposed research and literature is pivotal in any scholarly endeavor. It's crucial to understand the difference between these two types of employment in order to have a more complete understanding of the research subject. The purpose of this research is to address a variety of concerns, including creating mathematical models for the system, developing a efficient method for clustering flops with the same operations, and exploring effective methods for placing clocks and power gates in both active and idle modes. The investigation of the correct approach is for the integration of clock and power gating to attain enhanced performance. The primary goal of modern VLSI design is to optimize the circuit keeping in view the constraints i.e. Area, Timing, and Power. The discussed approach mainly focuses on either HDL-based implementation or software-based implementation for FPGAs. The approach is quite ineffective when it is considered a full custom or semi-custom IC design (6).

The proposed work mainly focused on these drawbacks. The proposed research work takes into consideration of Semi-Custom and Full custom IC design. The approach is based on deriving a power-efficient model which can fit the needs of both FPGA and ASIC designs.

METHODOLOGY

One of the most successful and commonly employed dynamic power reduction techniques is clock gating (7). The premise of this technique is that numerous transitions are extraneous and can be negated without any impact on the functionality of the circuit. Around 50% of the overall power of any processor is dynamic power which is predominantly due to system's clock. It is based on the observation that a large number of transitions in the circuit functionality are unnecessary. Such transitions can be suppressed without affecting functionality.

Clock signals play a critical role in the operation of VLSI (Very Large Scale Integration) chips by synchronizing the activities of various components within the chip. However, these clock signals also contribute to dynamic power consumption through several mechanisms, primarily due to the switching activity that occurs in response to each clock cycle.

One of the main contributors to dynamic power consumption in VLSI chips is the switching power associated with the clock signals. As the clock signal propagates through the chip, it triggers the sequential logic elements such as flip-flops and latches to transition between their states. This switching activity leads to dynamic power consumption as the internal node capacitances within these elements are charged and discharged with each clock cycle, resulting in energy dissipation.

Additionally, the clock distribution network in a chip also consumes power as it routes the clock signal to various parts of the chip. The buffers and wires used in the clock distribution network have parasitic capacitances that are charged and discharged with each clock cycle, contributing to overall power consumption in the chip. To mitigate the dynamic power consumption associated with clock signals, designers often employ clock gating techniques. Clock gating involves selectively enabling or disabling the clock signal to specific parts of the chip based on their activity level. When a particular block or functional unit is idle or not in use, the gating signal is activated to stop the clock signal from toggling in that region, thereby reducing unnecessary power consumption. The implementation of clock gating techniques offers several benefits, including significant power savings in idle or low-activity regions of the chip. (8)

By selectively gating the clock signal, designers can reduce dynamic power consumption and improve energy efficiency in the overall chip design. However, there is several trades-offs associated with the implementation of clock gating techniques:

1. Timing Closure: Implementing clock gating can introduce additional complexity to the design and may impact timing closure. Designers need to ensure that the gating signals are

generated and propagated correctly without causing timing violations, which can require additional design iterations and optimizations.

2. Design Overhead: Adding the logic required for generating gating signals and controlling clock signals can increase the design's area overhead and complexity. This additional logic may impact chip area, routing congestion, and overall design productivity.

3. Verification Complexity: Verifying a design with clock gating can be more challenging compared to a design without clock gating. Designers need to ensure that the gating signals are correctly generated and propagated under all operating conditions, which may require additional verification efforts and simulations.

4. Power-Aware Synthesis: Clock gating requires coordination between logic synthesis tools and clock tree synthesis tools to identify and insert gating elements effectively. This level of tool integration and optimization is crucial for maximizing the power savings from clock gating while ensuring design quality and performance.

The process of hardware/software co-design involves three main steps: clarification, modeling, design and validation (9). The first step is making specific and detailed models of the system, which describe the behavior of the system at a high level. The design process then proceeds in a step-by-step manner, utilizing multiple steps to transform the system's specifications into a practical application. This involves reducing the complexity of the system into simple blocks or tasks that implement the system's functionality. Ultimately, the cost step determines the cost parameters necessary for implementing the system's fundamental blocks in software or hardware. Several hardware parameters regarding cost are involved, including the number of gates, the area of the chip, and the power consumption. Conversely, software cost parameters include the time required for execution, the size of the code, and the amount of memory necessary for the code. Figure 1 shows a design flow for a typical co-design process. The depiction of the system is not reliant on either hardware or software, and assorted system representations could be utilized. Afterward, a programming language is used to describe the system, which is then compiled into an internal representation known as a data control flow description. This representation serves as a comprehensive system depiction that can represent both hardware and software. Partitioning the system is an iterative process, and if the evaluation fails to meet the objectives, another partition of hardware or software must be generated and assessed.

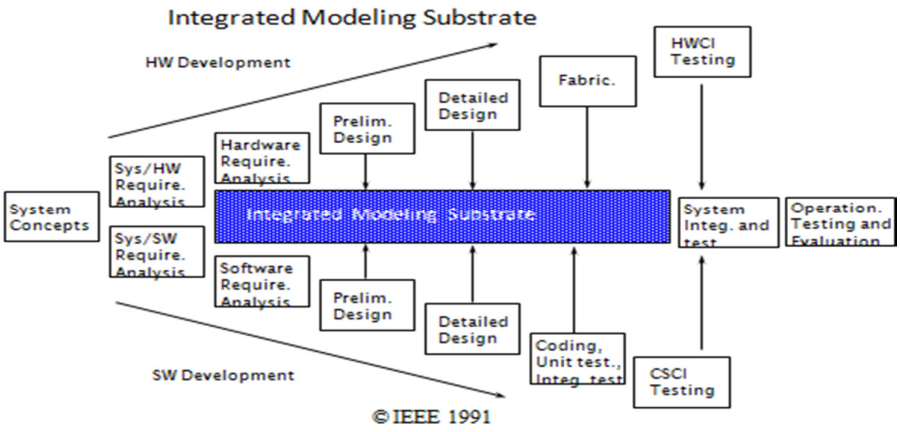

Figure 1: Directions of the HW/SW Design Process

Co-design is a vital approach utilized in the creation of embedded systems or SOC because of the inherent need for both hardware and software. Additionally, these systems are often crafted with cost and performance limitations in mind, which co-design can assist in meeting. To obtain filtered image, several cycles must be processed. During this process, certain design blocks become computationally intensive and slow down the overall performance of the encryption or decryption process. Due to its complicated and repetitive calculations, the HW/ SW co-design principle is best suited for the application of Median Filters (10),(11),(12).

Implementation of Median Filter using FPGA DE-2 board and NIOS-II

In order to validate research work undertaken, power-intensive systems are chosen based on their level of complexity. The implementation of power reduction methods for Median Filter is examined using three different approaches: hardware-only, software-only, and co-design. Implementation of Median Filter for these approaches using FPGA, NIOS-II and ASIC are analyzed in following sections where the application of clock gating for power reduction has been verified and the effectiveness of proposed methodology of integrating the clock gating with HW/SW co-design in the reduction of measurable amount of power has been observed.

Implementing a median filter using hardware-software co-design involves dividing the task between hardware and software components. Below is a simplified pseudo-code to illustrate this process. This pseudo-code presents a refined outline of the co-design approach:

Hardware Design (HDL - VHDL/Verilog) Pseudo Code

```
--Define the Input/Output Ports and Registers:
entity MedianFilter is
    Port (
        clk        : in std_logic;
        rst        : in std_logic;
        input_data : in std_logic_vector(7 downto 0);
        output_data: out std_logic_vector(7 downto 0)
    );
end MedianFilter;
--Define Internal Signals and Registers:
architecture Behavioral of MedianFilter is
    signal window : array(0 to 8) of std_logic_vector(7 downto 0);
    signal sorted_window : array(0 to 8) of std_logic_vector(7 downto 0);
    signal median : std_logic_vector(7 downto 0);
begin
--Shift Register for Sliding Window:
    process(clk, rst)
    begin
        if rst = '1' then
            for i in 0 to 8 loop
                window(i) <= (others => '0');
            end loop;
        elsif rising_edge(clk) then
            for i in 8 downto 1 loop
                window(i) <= window(i-1);
            end loop;
            window(0) <= input_data;
        end if;
    end process;
--Sorting Logic for Median Calculation:
    process(window)
    begin
    -- Implement sorting algorithm
         sorted_window <= bubble_sort(window);
        median <= sorted_window(4);
-- Middle element of sorted array
    end process;
--Assign the Median to Output:
    output_data <= median;
end Behavioral;
```

Software Design (C/C++ or SystemC) Pseudo Code

```
 // Define the Hardware Interface
#define INPUT_REG *((volatile uint8_t*) 0x0000) // Address of input register
#define OUTPUT_REG *((volatile uint8_t*) 0x0001) // Address of output register
// Main Software Loop:
int main()
 {
   uint8_t pixel;
   uint8_t filtered_pixel;
   while (1)
 {
 // Read pixel from image sensor or input source
       pixel = read_pixel();
 // Send pixel to hardware median filter
       INPUT_REG = pixel;
       // Wait for hardware to process
       wait_for_hardware();
       // Read filtered pixel from hardware
       filtered_pixel = OUTPUT_REG;
 / Write filtered pixel to output image or display
       write_pixel(filtered_pixel);
   }
   return 0;
}
// Utility Functions:
uint8_t read_pixel() {
 // Implementation to read a pixel from input source
   return input_pixel;
}
void write_pixel(uint8_t pixel)
{
   // Implementation to write a pixel to output destination
}
void wait_for_hardware()
 {
 // Implementation to wait for hardware processing to complete
// This could be a simple delay or checking a status register
}
```

The software reads pixel data from an input source. It sends the pixel data to the hardware median filter. After the hardware processes the data, the software reads the filtered pixel. The software then writes the filtered pixel to the output. The co-design of hardware and software is utilized to enhance and attain the optimal performance of an application or system. In order

to achieve this co-design, a series of steps were implemented to partition the system in a particular manner:

Partitioning

The co-design of hardware and software is utilized to enhance and attain the optimal performance of an application or system. In order to achieve this co-design, a series of steps were implemented to partition the system in a particular manner:

- The coding of the algorithm was done using ANSI C programming language.
- The NIOS-II processor was employed to rebuild and subsequently test this code.
- The duration of execution was gauged utilizing a stopwatch and quantified by the number of processor clock cycles.
- The VHDL language was utilized to implement intricate software components in hardware.

To decrease the volume of operations, a corresponding hardware arrangement is employed. This arrangement enables the simultaneous execution of operations.

Design steps for Median Filter

The following steps are used for the implementation of Median Filter with co-design technology.

- Development of hardware using SOPC builder
- Generation of VHDL code and .sof file in Altera
- Using the system-generated .ptf file in NIOS-II IDE tool
- Generation of C project using .ptf file
- Passing the inputs using software (C program) and getting the median value on the screen using NIOS-II Processor

The implementation of the Median Filter is focused solely on hardware design, both with and without the utilization of clock gating technique, on the FPGA DE-2 board. In order to achieve real-time output, the input and output devices of the FPGA DE-2 board are specifically assigned to I/O pins on the FPGA. Figure 4 displays the pin assignments and block diagram file for the implementation of the Median Filter in Quartus-II. Implementation of Median Filter using systolic architecture sort hardware technique on the soft core consists of two main units: Sort hardware accelerator (HW/MW) unit and Avalon Interface Unit. In the implementation of the hardware accelerator unit, insertion of data is mapped into the systolic array architecture. HW/MF consists of five processing elements to sort the nine

entries and finds the median value which is stored in the fifth processing element. The Processing Element is a composite of two tasks: comparison and right shifting. These tasks are carried out consecutively, one after the other, and each is completed within a single cycle of task execution.

The Avalon System Bus and HW/MF are able to transmit data by means of the Avalon Interface Unit. The Avalon Interface Unit has a design that is based on registers. It is composed of a multiplexer, a de-multiplexer, and several registers that are responsible for maintaining stable data. When data from the Avalon Bus is received, it is captured by the appropriate register based on the address that is supplied via the Address bus. Additionally, the Avalon Interface Unit produces a ONE-CLOCKCYCLE control signal that is required to activate the appropriate operation on HW/MF (11), (12).

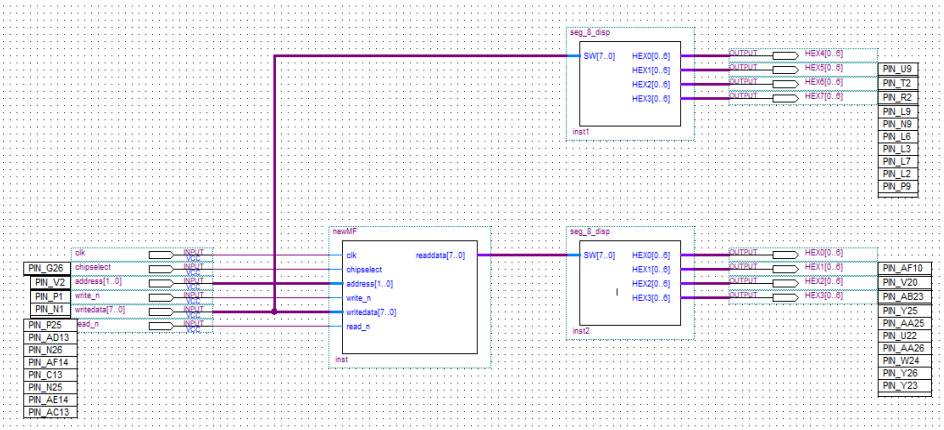

Figure 4: Pin assignment and block diagram file (bdf) of Median Filter for only hardware

In Figure 5, the power dissipation of the Median Filter is depicted without clock gating, while Figure 6 showcases the power dissipation with the inclusion of clock gating.

It is observed that, the static and I/O thermal power dissipation contributed more in the total power dissipation whereas the dynamic thermal power dissipation is very less 58.91 mW (26.48% of the total power) for without clock gating and 46.57 mW (22.18 % of the total power) for with clock gating. This is due to less switching activity of the signals.

The application of clock gating reduces a core dynamic thermal power dissipation of 20.95% though its impact on total power dissipation is very nominal to the tune of 5.58% only.

In generating the NIOS-II system, additional components like custom instructions and peripherals (e.g., SDRAM) are incorporated to accommodate its higher RAM requirements. In addition to the NIOS-II processor, the system is finalized by integrating it with other tailor-made peripherals. The system's block diagram can be seen in Figure 7.

PowerPlay Power Analyzer Status	Successful - Mon Jan 01 19:37:03 2024
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	median_soft
Top-level Entity Name	median_soft
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	222.44 mW
Core Dynamic Thermal Power Dissipation	58.91 mW
Core Static Thermal Power Dissipation	106.10 mW
I/O Thermal Power Dissipation	57.43 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 5: Power dissipation of Median Filter for only hardware design without clock gating technique using Cyclone-II

PowerPlay Power Analyzer Status	Successful - Mon Jan 01 19:41:42 2024
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	median_soft
Top-level Entity Name	median_soft
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	210.01 mW
Core Dynamic Thermal Power Dissipation	46.57 mW
Core Static Thermal Power Dissipation	106.01 mW
I/O Thermal Power Dissipation	57.43 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 6: Power dissipation of Median Filter for only hardware design with clock gating technique using Cyclone-II

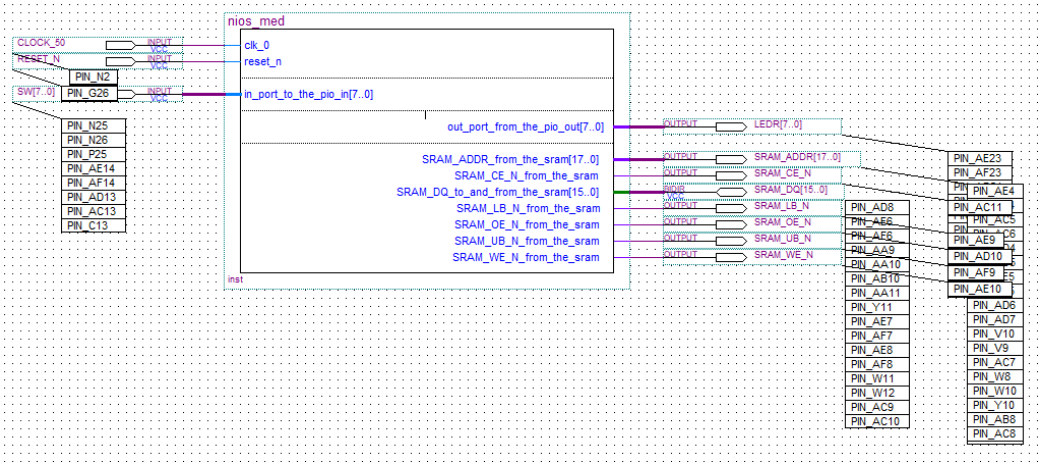

Figure 7: Block Diagram File (.bdf) of Median Filter for only software design

Power dissipation of Median Filter for only software design using NIOS-II is depicted in Figure 8 and Figure 9, for with and without clock gating. In Figure 8, the dynamic thermal power dissipation resulting from clock networking is measured at 3.72mW, while in Figure 9; the power dissipation reduces to 2.93mW with the implementation of clock gating. The software-based clock gating technique achieves a dynamic power reduction of 21.24% and a total power reduction of 0.84%.

PowerPlay Power Analyzer Status	Successful - Mon Jan 01 19:32:29 2024
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	median_dump
Top-level Entity Name	median_dump
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	179.54 mW
Core Dynamic Thermal Power Dissipation	3.72 mW
Core Static Thermal Power Dissipation	105.55 mW
I/O Thermal Power Dissipation	70.27 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 8: Power dissipation of Median Filter for only software design without clock gating technique using NIOS-II

PowerPlay Power Analyzer Status	Successful - Mon Jan 01 19:29:40 2024
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	median_dump
Top-level Entity Name	median_dump
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	178.04 mW
Core Dynamic Thermal Power Dissipation	2.93 mW
Core Static Thermal Power Dissipation	105.54 mW
I/O Thermal Power Dissipation	69.56 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 9: Power dissipation of Median Filter for only software design with clock gating technique using NIOS-II

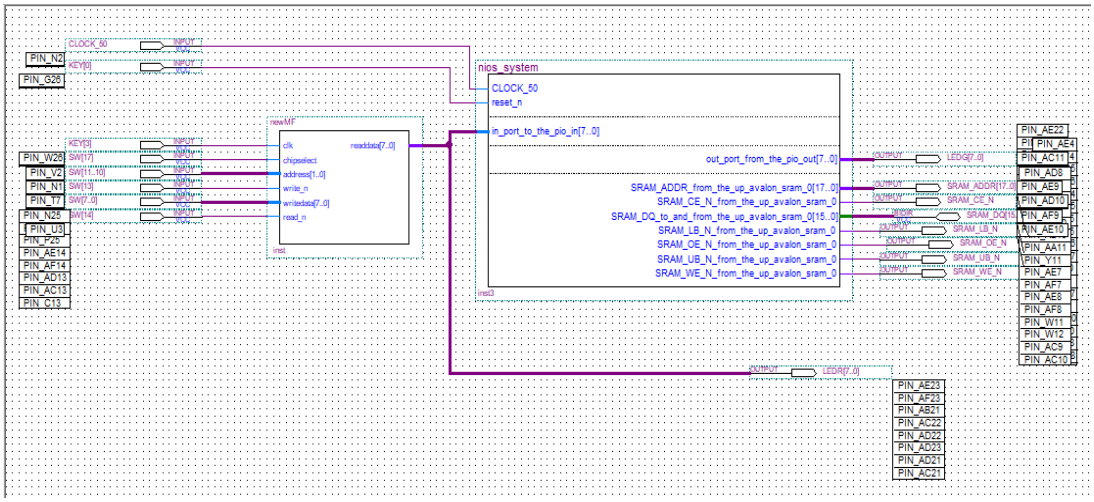

Figure 10: Block Diagram file (bdf) for Median Filter Co-design

Figure 10 shows Block Diagram file (bdf) of Median Filter with Co-design technique. The first block indicates Avalon Interface unit and the second indicates the Processing Elements (PE). At the 1st clock pulse; reset is done assigned to '0' at address '0'. At the 2nd clock

pulse, writep is assigned '1' at address '1'. At the 3rd clock pulse, writedatap is passed to HW/MF at address '2' for two clock pulses. The completion of the INSERT operation requires two clock cycles for the Processing Element. Signal writeP must be asserted after writedataP has been presented at least one Clock Cycle earlier. The input control signal, writeP asserted for one clock in falling edge clock event. The signals writedataS and PEstorage are asserted for two clocks in rising edge clock event. The median value in PEstorage5 only valid at least after nine clocks of last input data i.e. 9th data inserted as shown in Figure 10. The median value is obtained after 28th clock pulse.

PowerPlay Power Analyzer Status	Successful - Mon Jan 01 19:47:06 2024
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	median_custom
Top-level Entity Name	median_custom
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	230.27 mW
Core Dynamic Thermal Power Dissipation	61.43 mW
Core Static Thermal Power Dissipation	105.87 mW
I/O Thermal Power Dissipation	62.97 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 11: Power dissipation of Median Filter using Co-design method with clock gating technique using Cyclone-II and NIOS-II

PowerPlay Power Analyzer Status	Successful - Mon Jan 01 19:51:44 2024
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	median_custom
Top-level Entity Name	median_custom
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	219.96 mW
Core Dynamic Thermal Power Dissipation	51.19 mW
Core Static Thermal Power Dissipation	105.80 mW
I/O Thermal Power Dissipation	62.97 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 12: Power dissipation of Median Filter using Co-design method with clock gating technique using Cyclone-II and NIOS-II

Figure 11 and 12 illustrate the power consumption of the Median Filter in both the co-design method with and without applying the clock gating technique in an FPGA-based approach. The utilization of clock gating technology resulted in a significant reduction in core dynamic power and total thermal power, achieving a decrease of 16.67% and 4.48% respectively. To further analyze the power dissipation of these designs, the same co-designs with and without clock gating technology were implemented using the 90 nm IBM CMOS library. Figure 6.45 showcases the power dissipation of the Median Filter through the HW/SW co-design approach with clock gating technology in an ASIC approach, providing more specific

insights into power dissipation. By comparing the power consumption data provided in Figures 5 and 6, Figures 8 and 9, and Figures 11 and 12, as well as Figure 13, for systems designed using FPGA and NIOS-II, the following observations made for different approaches such as hardware only, software only, HW/SW co-design, and HW/SW co-design with clock gating technology in the ASIC approach.

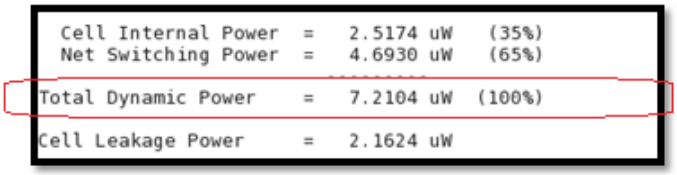

Figure 13: Power dissipation of Median Filter by HW/ SW Co-design with clock gating technology in ASIC approach

The power consumption for the Median Filter system, excluding clock gating, varies depending on the design approach. The hardware-only design consumes 222.44 mW, the software-only design consumes 179.54 mW, and the HW/SW co-design consumes 230.27 mW. Notably, the software-only design utilizing NIOS-II exhibits the lowest power consumption compared to all other designs. For hardware-only design, the consumption of dynamic thermal power amounts to 58.91 mW, while software-only designs consume 3.72 mW. In the case of HW/SW co-design, the dynamic thermal power consumption reaches 61.43 mW.

The implementation of clock gating has proven to be effective in reducing the consumption of dynamic thermal power. After incorporating clock gating into the aforementioned designs, the dynamic thermal power consumption values were measured at 46.57 mW, 2.93 mW, and 51.19 mW for the hardware-only design, software-only design, and HW/SW co-design, respectively. This corresponds to a percentage saving of 20.94%, 21.23%, and 16.66% for the hardware-only design, software-only design, and HW/SW co-design, respectively. The implementation of clock gating in the co-design process resulted in a significant decrease of 13.1% in dynamic power dissipation compared to a hardware-only design. The implementation of clock gating has resulted in a decrease in overall power dissipation. Specifically, the power consumption for hardware-only design, software-only design, and HW/SW co-design has been reduced to 210.01 mW, 178.04 mW, and 219.96 mW respectively. This represents a reduction of 5.59%, 0.83%, and 4.45% for hardware-only design, software-only design, and HW/SW co-design, respectively. Additionally, the overall power consumption was reduced by 1.11% when transitioning from a hardware-only design

to a co-design with clock gating.

By employing a combination of hardware and software co-design, along with clock gating technology, the ASIC approach has demonstrated total dynamic power dissipation of 7.2104 uW which is very less as compared to the FPGA based design.

This co-design approach leverages the parallel processing capabilities of hardware for the computationally intensive task of median filtering, while the software manages data flow and control, ensuring efficient and flexible implementation. To emphasis power reduction by the proposed methodology, the design is ported into ASIC 90 nm CMOS IBM library. The design is synthesized using Synopsis tool and estimated the power consumption of both methods; with and without clock gating technique.

RESULT and DISCUSSION

The proposed methodology employed both clock gating and Co-design as a significant high-level technique for reducing the power consumption of a design. The process of clocking reduces the power dissipation of the clock network, relaxing the data path's timing, and decreases the congestion of the routing by eliminating feedback loops that multiplex information (14). The Co-design technique reduces overall power consumption with increase in performance. Design Compiler gives the detailed information about the static and dynamic power. A digital ASIC implementation of the hardware-software co design results in constant, consistent and a high performing circuit design, while the power optimized Hardware Software co-design style leads to Power efficient architecture. The major goal of research methodology is to become aware of an appropriate design for making use of proposed methodology. Median filter systems are based on a design concept known as a substitution–permutation network which desires to go-through many rounds to generate the cipher text. During this process, there are few blocks that are computationally in-depth and sluggish down overall performance and thus the encryption/Decryption method. So, the proposed technique is excellently suited for the application of the HW/ SW co-design principle. To prove the individuality of proposed methodology, the systems were prototyped on FPGA then as a part of SoC design, the same designs were ported into 180nm IBM library. Further reduction in dynamic power is achieved by invoking clock gating using Synopsys tool called the “Design Compiler.

Tables 1 to Table 5 are highlighting the comparative analysis of various design parameters of median filter by implementing FPGA and ASIC based approaches respectively.

The power dissipation of the Median Filter is displayed in Tables 1 and 4, showcasing the

results for both the implementation without clock gating technology and the implementation with clock gating technology using an FPGA-based approach at a frequency of 50MHz.

Table 1: Power dissipation of Median Filter for without clock gating technology using FPGA based approach

Design Type Without CG	Core Dynamic Thermal Power mW	Core Static Thermal Power mW	I/O Thermal Power mW	Total Thermal Power Dissipation in mW
Hardware only	58.91	106.1	57.43	222.44
Only NIOS-II	3.72	105.55	70.27	179.54
HW/ SW Co design	61.43	105.87	62.97	230.27

Table 2: Power dissipation of Median Filter for with clock gating technology using FPGA based approach

Design Type With CG	Core Dynamic Thermal Power mW	Core Static Thermal Power mW	I/O Thermal Power mW	Total Thermal Power Dissipation in mW
Hardware only	46.57	106.01	57.43	210.01
Only NIOS-II	2.93	105.54	69.56	178.04
HW/SW Co design	51.19	105.8	62.97	219.96

Table 3 represents comparative analysis of power dissipation of Median Filter for with and without clock gating technology using FPGA based approach. It is evident from the Table 3 that, dynamic power reduction by applying clock gating for only hardware, only software and HW/SW co-design is 20.95%, 21.24% and 16.67% respectively. Due to constant static power dissipation for all three designs, and total power reduction observed is of 5.59%, 0.84% and 4.48%. The data reveals a decrease of 13% in core dynamic thermal power and a decrease of 1.11% in total thermal dissipation. Table 4 reflects that, there is a minimal effect on the utilization of logic cells for implementation of Median filter with clock gating. However, as the number of logic elements utilized by the Median Filter increased by 3%, the delay increased by 17 %.

Table 3: Comparative analysis of power dissipation of Median Filter for with and without clock gating technology using FPGA based approach

Design Type	Dynamic Power mW (without Clock Gating)	Dynamic Power mW (with Clock Gating)	% reduction in Dynamic Power mW With application of Clock gating	Total Power mW (without Clock Gating)	Total Power mW (with Clock Gating)	% reduction in Total Power mW With application of Clock gating
Hardware only	58.91	46.57	20.95%	222.44	210.01	5.59%
Only NIOS-II	3.72	2.93	21.24%	179.54	178.04	0.84%
HW/ SW-Co-design	61.43	51.19	16.67%	230.27	219.96	4.48%

Table 4: Comparison of Logic Cells utilization and Critical path register to register delay for Median Filter using FPGA based approach

Design Type	Without CG		With CG	
	Logic Cells utilization	Critical path register to register delay	Logic Cells utilization	Critical path register to register delay
Hardware only	3984 (12%)	10.589 ns	3588 (10.8%)	11.686 ns
Only NIOS-II	395 (1.2%)	4.305 ns	407 (1.22%)	3.662 ns
Hardware-Software Co-design	4567 (13.6%)	10.903 ns	4122 (12.4%)	12.415 ns

Table 5: Power dissipation of Median Filter for ASIC approach

Design Type	ASIC Approach (Dynamic Power)
Hardware only	14.2567 μW
Only NIOS-II	12.3546 μW
HW/ SW-Co design with CG	7.2104 μW

Figure 14 shows dynamic power reduction of Median Filter by clock gating using FPGA based Approach. The power dissipation of the Median Filter using the IBM 90 nm library for only hardware as well as for software without clock gating and co-design with clock gating designs is demonstrated in Table 5. It is evident that the power dissipation values are in the range of μW which depicts that the implementation of FPGA in ASIC form results in drastic reduction in the power consumption. Furthermore the use of clock gating integrated with co-

design results in the smallest amount of power consumption. When considering power dissipation for the ASIC based design, a system's total power consists of two distinct elements: dynamic power and static/leakage power. The measurement of static power dissipation is greatly influenced by the technology employed. It is evident that the leakage/static power dissipation is in the range of μW, while the switching or dynamic power dissipation is in the range of mW. However, as technology advances beyond ηm, the impact of leakage power dissipation may become more significant, eventually surpassing dynamic dissipation as the primary contributor to overall power dissipation.

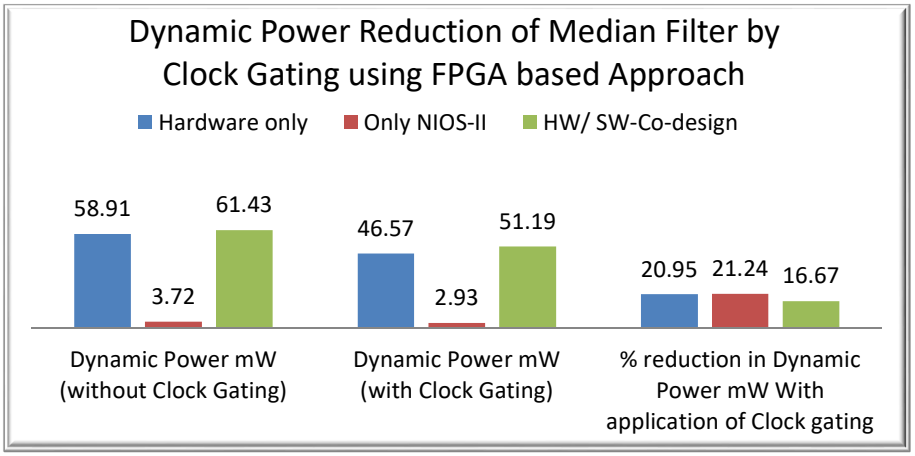

Figure 14: Dynamic Power reduction of Median by Clock Gating using FPGA based Approach

The development of improved power-efficient techniques for FPGA based systems using co-design and clock gating, especially when integrating ASIC components, is a complex and valuable endeavor. The research work aimed to enhance the power efficiency of FPGA based systems by combining co-design strategies and clock gating techniques, specifically when integrating ASIC components.

From extensive experimentation (Tables 1-2, 5, 7-9, 12), it is inferred that proposed method is a competitive power reduction technique in digital circuits implementing using FPGA. Certain analysis (Tables 3-4, 6, 10-11) also illustrates the importance of logic elements and critical delay between the registers for improving quantitative results. The statistical analysis shows that proposed technique has improved reduction in overall power dissipation by 94%

Abbreviations

Nil

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Author contribution

Padmini Gowrang Kaushik: Conceptualization, methodology, background work, dataset collection, implementation, result analysis and comparison, preparing and editing draft and visualization.

Sanjay M. Gulhane: Supervision, background work, review of the work, project administration, and editing draft.

Conflicts of interest

The authors have no conflicts of interest to declare.

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