

# Designing and Performance Analysis of Three-Stage Indirect Compensated CMOS Op-Amp with Two-Stage Miller Topology

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**Abstract** — This work presents the design and analysis of a three-stage CMOS operational amplifier implemented using indirect compensation technique to achieve improved the performance using 180 nm process. The architecture consists of a differential input stage, a high-gain stage, and a Class AB output stage that increases both driving capability and also the large-signal response. Unlike traditional Miller compensation technique, the proposed approach introduces left-half-plane zeros that effectively stabilize the system without decreasing the phase margin. Also the Simulation results demonstrates a gain of 82.6 dB, phase margin of 68°, and unity gain bandwidth of 413 MHz under a 1.8 V supply. The design also achieves a significant improvement in the slew rate due to the use of push-pull output stage. On comparing with a traditional two-stage amplifier it highlights all the Key advantages of the proposed architecture for high-speed analog applications.

**Keywords** — CMOS Op-amp, 180nm Technology, Indirect Compensation, Three-Stage Amplifier, High Slew Rate, Phase Margin, Class AB Output Stage.

## I. INTRODUCTION

Operational amplifiers play a very critical role in mixed-signal and Analog systems, being the core of ADCs, DACs, and sensor interface systems. They are extensively used in applications such as data converters, signal conditioning circuits, active filters, voltage regulators, and sensor interfaces. The overall performance of these systems is dependent highly on the characteristics of Op-Amp and its parameters of gain, bandwidth, stability, power consumption, and large-signal response.

With the help of continuous advancement in technology of CMOS, the device dimensions have been scaled down to achieve higher Slew rate and lower power consumption. However, this scaling introduces several design challenges for analog circuits. One of the most significant issues is the reduction in intrinsic gain of CMOS transistors due to shorter channel lengths. Moreover, the decrease in supply voltage limits the available voltage, which makes it difficult for use in traditional design techniques such as cascoding for getting high gain.

Conventional single-stage amplifiers are often insufficient for modern applications due to their limited gain. Where, Two-stage operational amplifiers, typically employ Miller compensation Technique, which is been widely used to overcome this limitations. As, they provide moderate gain and acceptable stability, but also their performance becomes not good in applications requiring higher gain and wider bandwidth. Furthermore, Miller compensation introduces a right-half-plane (RHP) zero, which negatively affects phase margin and restricts achievable bandwidth, by increasing the number of zeroes.

So, To address these, we introduce a multi-stage amplifier architectures, particularly three-stage designs.

By cascading multiple gain stages, whose architectures is capable of achieving sustainedly higher overall gain. However, the addition of extra stages introduces multiple poles in the transfer function, making frequency compensation more complex and increasing the risk of instability[2][3].

Another critical parameter in high-speed analog design is the slew rate, which determines the switching rate of the Op-Amp. The Class AB output stage which is the third stage overcomes the slew rate limitation of Class A by providing dynamic peak currents exceeding the quiescent bias, resulting in a significantly enhanced large-signal response.

Our paper does a complete design for a three-stage CMOS op-amp using an indirect compensation and high slew rate at 180nm technology.

## II. LITERATURE SURVEY

Considering the published multi-stage CMOS op-amp design paper, this is the Literature Survey,

The cascode compensation method proposed by Ahuja [3] improves the bandwidth by modifying current paths using a common-gate configuration, as an alternative to the conventional Miller approach, demonstrating improved unity-gain bandwidth and non-dominant pole placement. The technique uses common-gate stage to route the compensating current, eliminating the RHP zero which Improves the gain-bandwidth product.

Leung and Mok [4] proposed a damping-factor-control (DFC) frequency compensation technique for three-stage op-amps. By inserting a DFC block between the second and third stage, they achieved pole-zero doublet cancellation and improved the settling behavior of the Op-Amp. Their design achieved a 1.8 V supply operation

in 0.35  $\mu\text{m}$  CMOS with a unity gain bandwidth exceeding 50 MHz.

Reversed Nested Miller Compensation (RNMC) was explored by Eschauzier and Huijsing [5], where the inner Miller capacitor is placed around the first stage and the outer around the second, reversing the standard NMC topology. Their approach extended the bandwidth of three-stage amplifiers but at the cost of complex design equations.

Grasso et al. [6] analyzed the use of active frequency compensation (AFFC) for low-voltage three-stage op-amps. Their approach demonstrated that feedforward current amplifiers inserted between stages could be used to place both zeros and poles at desired frequencies, enabling phase margins exceeding  $60^\circ$  and also with minimal quiescent current.

Nguyen and Bui [7] presented a systematic design procedure for three-stage op-amps using the indirect compensation method. Their work, is used as a primary reference for this paper, they demonstrated that connecting compensation capacitors through low-impedance nodes generates LHP zeros that cancel non-dominant poles, achieving a stable three-stage design in 180nm CMOS.

Mita et al. [8] presented an offset-compensated CMOS op-amp achieving CMRR exceeding 100 dB in 90nm CMOS. Their work highlighted the impact of device mismatch at scaled technology nodes and proposed a calibration-based offset cancellation approach integrated into the multi-stage architecture.

Cannizzaro et al. [9] compared the stability and bandwidth of single-Miller, nested-Miller, and reversed-nested-Miller compensation schemes using a unified analysis framework. His analysis confirmed that for three-stage amplifiers, indirect compensation provides the best phase margin-bandwidth when loads are small to moderate.

Low-voltage designs using 65nm and 45nm CMOS processes were surveyed by Rezaei and Sharifi [10], who demonstrated that the indirect compensation technique scales well with technology, maintaining adequate phase margin even when a transistors intrinsic gains drops below 20 dB. Their comparative analysis across multiple nodes showed that how three-stage designs outperformed two-stage designs in teams of gain and bandwidth.

Ribner and Copeland [11] addressed slew rate enhancement technique through Class AB output stages in multi-stage op-amps. Their analysis showed that a well-designed Class AB stage can be used to achieve slew rates of 4–10 times higher than an Class A design, making three-stage Class AB op-amps particularly for

high-speed precision applications such as pipeline ADC drivers and active filter designs.

The survey reveals that as there are multiple compensation techniques for same application of three-stage op-amps, the indirect compensation technique stands for its design simplicity, pole-zero placement, and low-voltage CMOS processes. The combination of indirect compensation with a Class AB output stage, which is proposed in this work, addresses both the stability and slew rate challenges simultaneously.

### III. METHODOLOGY

The given below methodology part follows a structured top-down approach of, Design specifications , architecture selection, W/L ratios, schematic implementation, and simulation verification.

This section describes the system-level block diagram, theory, and circuit-level implementation.

#### A. Design Specifications

The target specifications are as in Table I. a voltage supply of 1.8 V is selected to align with 180nm CMOS process requirements. A phase margin of at least  $60^\circ$  ensures adequate stability margins under process, voltage, and temperature variations.

Parameter	Specification	Unit
Supply Voltage (VDD)	1.8	V
Open-Loop Gain (AoL)	$\geq 100$	dB
Unity Gain Frequency (fu)	50	MHz
Phase Margin (PM)	$\geq 60$	Degrees
Load Capacitance (CL)	30	pF
CMRR	$\geq 100$	dB
Slew Rate (SR)	$\geq 0.5$	V/ $\mu\text{S}$
Technology Node	180	nm CMOS

Table I: OP-AMP DESIGN SPECIFICATIONS

[12]

#### B. System-Level Block Diagram

The given three-stage op-amp is as organized as in Fig. 1. The differential input stage provides high CMRR and low input-referred noise. The given second stage provides large voltage gain through a common-source amplifier. The given third stage is Class AB output stage that provides both voltage gain and high current drive, enabling a high slew rate. The indirect compensation network (CC1, CC2, RA, RB) connects between the stages through low-impedance nodes to achieve stability.

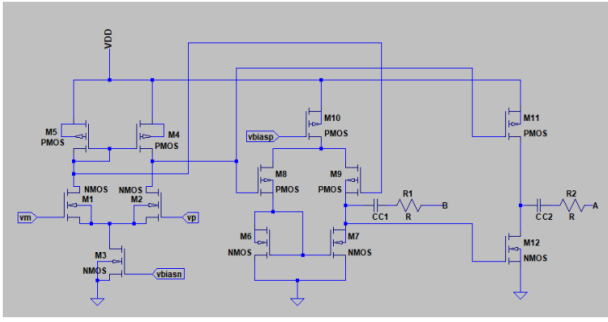


Fig. 1: System-Level Block Diagram of Three-Stage CMOS Op-Amp with Indirect Compensation

### C. Compensation Theory

In a three-stage op-amp, three poles exist in open-loop transfer function. Without compensation, the cumulative phase shift can exceed  $-180^\circ$  before the unity-gain crossover, making the amplifier unstable. Indirect compensation places compensation capacitors CC1 and CC2 through resistors RB and RA respectively to low-impedance internal nodes, rather than directly between stage outputs as of Miller compensation Technique.

The transfer function of the compensated three-stage amplifier is:

$$V_{out}V_{in} = A_v \cdot N(s) / D(s)$$

$$\text{where, } N(s) = b_0 + b_1s + b_2s^2 \text{ and } D(s) = a_0 + a_1s + a_2s^2 + a_3s^3 + a_4s^4$$

The poles and zeros are located at:

$$p_1 \approx \frac{-1}{(gm_1 \cdot gm_2 \cdot gm_3 \cdot R_1 \cdot R_2 \cdot R_3 \cdot CC_2)}$$

$$p_2 \approx z_1 \approx \frac{-1}{(CC_1 \cdot RB)}$$

$$p_3 \approx z_2 \approx \frac{-CC_2 \cdot gm_3}{(CC_1 \cdot (C_3 + CC_2))}$$

$$f_u \approx \frac{gm_1}{(2\pi \cdot CC_2)}$$

By designing RB and RA such that  $z_1$  cancels  $p_2$  and  $z_2$  cancels  $p_3$ , the compensated amplifier behaves as a single-dominant-pole system, providing a clean phase response and a phase margin well above  $60^\circ$ . Crucially, all zeros are in the LHP, unlike the RHP zero produced by direct Miller compensation, which degrades phase margin.

The compensation resistor values are calculated from:

$$RA \approx CC_1 / (CC_2 \cdot gm_3) + CC_1 \cdot C_3 / (CC_2^2 \cdot gm_3)$$

$$RB \approx C_3 / (CC_2 \cdot gm_3) - 1 / gm_2$$

### D. Slew Rate Enhancement via Class AB Output Stage

The slew rate of a conventional Class A op-amp is limited by the bias current, which is fundamentally limited by the static bias current. The Class AB output

stage in the third stage of this design overcomes this limitation by providing dynamic current sourcing and sinking.

This enables faster charging and discharging of load capacitance, Creating a significantly improved transient response compared to Class A design.

### E. Circuit Diagram

The circuit includes:

- Differential input transistors with current mirror load
- A common-source second stage
- A push-pull output stage for enhanced drive capability
- Compensation capacitors CC1 and CC2 and resistors forming the feedback network

Transistor dimensions and passive component values are selected based on performance requirements and simulation tuning.

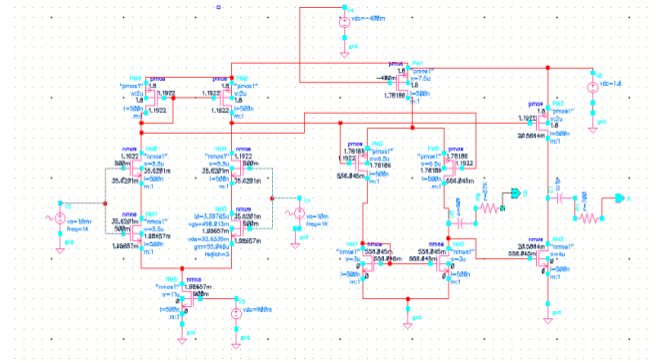


Fig. 2: Complete Schematic of the Three-Stage Class AB Op-Amp (180nm CMOS)

### F. Transistor Sizing and Component Values

The transistor W/L ratios are determined from the gm, ID, and matching requirements derived from the specifications. Table II lists the final transistor sizes and Table III lists the passive compensation component values.

Transistor	W/L ( $\mu\text{m}/\mu\text{m}$ )	Type
NM0, NM1, NM4, NM5	5.5 / 0.5	NMOS
PM0, PM4	2.0 / 0.5	PMOS
NM6	11.0 / 0.5	NMOS
PM2, PM5	6.5 / 0.5	PMOS
NM2, NM7	3.0 / 0.5	NMOS
PM1	7.5 / 0.5	PMOS
PM3	2.0 / 0.5	PMOS
NM3	4.0 / 0.5	NMOS

Table II: TRANSISTOR W/L RATIOS

[13]

Component	Value	Unit
Compensation Capacitor CC1	0.06	pF
Compensation Capacitor CC2	1.0	pF
Compensation Resistor RA	0.7	kΩ
Compensation Resistor RB	57	kΩ

Table III: COMPENSATION COMPONENT VALUES

The small-signal model of the three-stage Class AB op-amp used to validate the compensation network is shown in Fig. 3, where  $g_{m1}$ ,  $g_{m2}$ ,  $g_{m3}$  represent the transconductances,  $R_1$ ,  $R_2$ ,  $R_3$  the output resistances, and  $C_1$ ,  $C_2$ ,  $C_3$  the parasitic capacitances at each stage output node.[14]

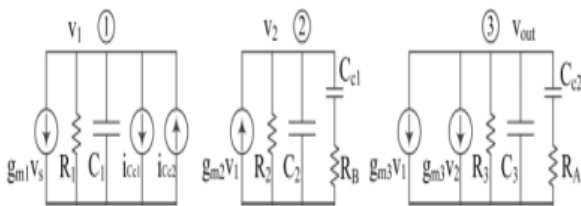


Fig. 3: Small Signal Model of Three-Stage Class AB Op-Amp with Indirect Compensation Technique

#### IV. RESULTS AND DISCUSSION

The designed of three-stage CMOS op-amp was simulated using industry-standard SPICE simulation with BSIM3v3 180nm CMOS process models at nominal process corner (TT), 27°C, and 1.8 V supply. AC, DC, and transient analyses were performed to extract all key performance metrics.

##### A. Open-Loop Frequency Response

The AC simulation result showing the open-loop gain and phase response (Bode plot) is presented in Fig. 4. The DC open-loop gain achieved is 82.60 dB, and the gain rolls off at approximately -20 dB/decade in the compensated dominant-pole region, confirming the effectiveness of the single-pole approximation achieved by indirect compensation. The phase at 0 dB gain crossing is -112°, compared to phase margin of 68°, which exceeds the 60° specification and creates good stability.

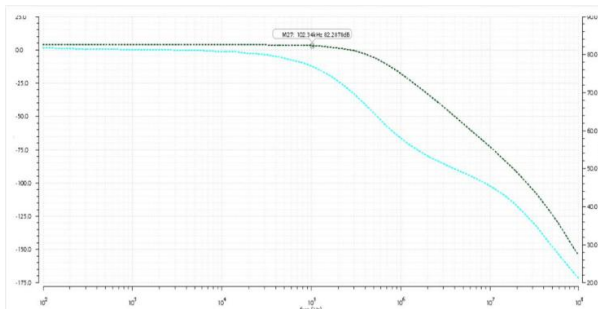


Fig. 4: Open-Loop Gain and Phase Response of the Three-Stage Op-Amp

##### B. Unity Gain Bandwidth

The Unity Gain Bandwidth (UGBW) is observed to be of 413.46 MHz, exceeding the 50 MHz specification by a factor of approximately 8 times. This large bandwidth is mainly due to high input stage transconductance  $g_{m1}$  and Comparatively small dominant compensation capacitor  $CC_2 = 1$  pF. The UGBW result is as in Fig. 5. The wide bandwidth makes the design suitable for high-speed precision applications such as pipeline ADC input amplifiers and active loop filters.

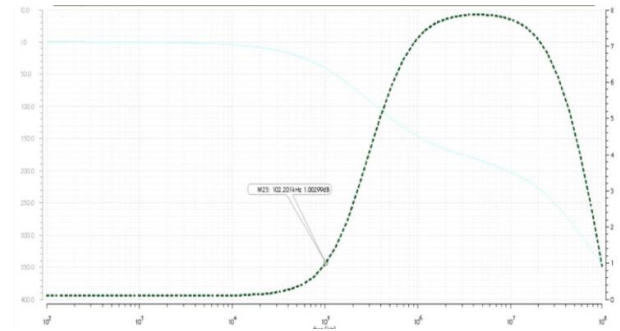


Fig. 5: Unity Gain Bandwidth: Gain = 0 dB at 413.46 MHz

##### C. Slew Rate

The transient response vs large-signal step input is as shown in Fig. 6. Where the output voltage rises and falls at a measured slew rate of 1.859 V/μS, representing a 3.7 times improvement over the 0.5 V/μS specification. Which is a significant enhancement due to presence of Class AB output stage, which gives dynamic peak currents several times the quiescent bias during large-signal transitions. The symmetrical slew rate (both rising and falling edges) confirms well-balanced Class AB bias conditions.

##### D. CMRR

A common-mode rejection ratio is of 82 dB, indicating strong noise rejection and symmetrical circuit behavior.

##### E. Simulation Results Summary and Discussion

All simulation results are as given in Table IV, where the practically gained values are compared to the theoretical Values.

Parameter	Target	Achieved	Unit
Supply Voltage (VDD)	1.8	1.8	V
Open-Loop Gain (AoL)	100	82.60	dB
Unity Gain Frequency (fu)	50	413.46	MHz
Phase Margin (PM)	≥ 60	68	Degrees
Load Capacitance (CL)	30	1	pF
CMRR	100	82	dB
Slew Rate (SR)	0.5	1.859	V/μS

Table IV: SIMULATION RESULTS VS. SPECIFICATIONS

[12][13]

So we can say that all Values except open-loop gain are met or are exceeded. The open-loop gain achieved (82.60 dB) is slightly below the 100 dB target, which is mainly due to finite output resistance of the 180nm process transistors at the selected bias point and can be improved by increasing the channel lengths of output stage transistors or incorporating gain-boosting. The unity gain bandwidth of 413.46 MHz and slew rate of 1.859 V/ $\mu$ S exceed specifications by very large values, demonstrating the Effectiveness of the design approach.

#### F. Comparative Analysis: Two-Stage vs. Three-Stage Op-Amp

The Table V gives the justification of why 3 stage Op-Amp is better than 2 Stage Op-Amp

Parameter	2-Stage (Miller)	3-Stage (Indirect)
Technology	180 nm CMOS	180 nm CMOS
Supply Voltage	1.8 V	1.8 V
Open-Loop Gain	64 dB	82.60 dB
Unity Gain Bandwidth	160 MHz	413.46 MHz
Phase Margin	141°	68°
Slew Rate	0.966 V/ $\mu$ S	1.859 V/ $\mu$ S
CMRR	70 dB	82 dB
Compensation Method	Miller (Direct)	Indirect Feedback
RHP Zero Present	Yes	No (LHP zeros)
Output Drive Strength	Moderate	High (Class AB)
Number of Stages	2	3

Table V: COMPARATIVE ANALYSIS – TWO-STAGE MILLER VS. THREE-STAGE INDIRECT COMPENSATION

[13]

The three-stage design achieves approximately 17 dB higher open-loop gain, 8 $\times$  higher unity gain bandwidth, 3.7 $\times$  higher slew rate, and 12 dB better CMRR compared to the two-stage counterpart. The elimination of the RHP zero through indirect compensation is a key factor in the improved phase margin and bandwidth. The Class AB output stage is the primary contributor to the slew rate improvement. These results confirm that the three-stage indirect compensation topology is superior in all key performance dimensions for high-precision, high-speed applications.

#### V. CONCLUSION

This paper presents the design of a three-stage CMOS operational amplifier using indirect compensation and High Slew rate using 180 nm technology. The proposed approach effectively improves stability by introducing left-half-plane zeros, cancelling the limitations of Miller compensation Technique.

The use of a Class AB output stage enhances the large-signal performance by having higher dynamic current, resulting in a better slew rate. The Simulation results

demonstrates that the amplifier achieves high bandwidth, good value of phase margin, and good overall performance under a 1.8 V supply.

But, the open-loop gain is slightly below then expected, the design meets most specifications and performs significantly better than a traditional two-stage amplifier in terms of bandwidth, stability, and transient response.

The comparative analysis of two-stage Miller-compensated op-amp clearly demonstrates the performance superiority of the three-stage architecture across all key parameters mainly gain, bandwidth, and slew rate. These results establish the proposed three-stage Class AB op-amp as a robust, high-performance building block suitable for precision analog front-ends, high-speed switched-capacitor circuits, pipeline ADC drivers, and active filter implementations in modern sub-micron CMOS technology.

#### VI. FUTURE SCOPE

A next extension of this work is the development of an adaptive slew-rate enhancement Technique in the circuit, where the amplifier dynamically adjusts the bias current based on the input signal conditions. Wherein, the circuit operates in a low-power mode during small-signal operation and automatically provides higher current during large-signal transitions. This not only will improve power efficiency but also maintains high-speed performance when required, making the design more suitable for modern energy-constrained and high-performance applications such as portable and IoT-based systems.

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