STANDARD SKELETON CELL FOR STANDARD CELL DESIGN

Bala Iyyappan M S
Department of Electronics and Communication Engineering
National Engineering College, Kovilpatti, India

Subramanian K
Department of Electronics and Communication Engineering
National Engineering College, Kovilpatti, India

Abstract **- In modern-day IC technology, the number of transistors used in a single IC is countless based on application. The higher the circuit complexity, the more complex routing and placement become, so routing a transistor with that much area is time-consuming. So, we use various tools to automate routing and placement. Another problem arises when we are using CMOS technology is the standardized cell without any constraints. By seeing it on one side it gives as an advantage, but on the other side if we want an inverter of 2 times its drive strength, for that we need two standard cell inverters one by one or by fabricating an actual two times of a unit width. It is very area consuming, and it also increases the use of metals and so is the delay. As a result, fingers can be used to overcome this problem. By using the finger concept, the area is really decreased. This can be avoided by using standard grid cells which have the advantage of repeatability and automated layout tools like placement and routing in CMOS technology. These standard cells will have a standard height and variable width. In this work, efforts are made to create a standard skeleton cell for automation and repeatability.**

Keywords: IC, CMOS, Standard grids and Skeleton cells

I. INTRODUCTION

A standard grid cell stands as a foundational building block, essential for the creation and development of diverse circuits adhering to CMOS (Complementary Metal-Oxide Semiconductor) logic, which serves as a fundamental framework for contemporary integrated circuits. At the core of CMOS logic lie PMOS (P-type Metal-Oxide-Semiconductor) and NMOS (N-type Metal-Oxide-Semiconductor) transistors, operating in a complementary and symbiotic manner. This symbiosis is instrumental in engineering efficient, low-power, and high-performance circuitry, embodying the essence of modern electronic applications. The subsequent discourse delves into an in-depth exploration of the functionalities and applications of PMOS and NMOS transistors within the CMOS logic paradigm. It emphasizes their complementary behavior, illustrating how PMOS transistors handle the "true" logic functions while NMOS transistors manage the inverse or "complementary" aspects. The discussion also sheds light on their crucial roles in logic level implementation, elucidating how PMOS transistors facilitate logic high (1) when the input is at logic low (0) and vice versa for NMOS transistors. Further insight is provided into the nuanced mechanics of CMOS inverters, where PMOS and NMOS transistors operate as pull-up and pull-down devices, respectively, shaping the output based on the input signal. The description extends to encompass diverse logic gates, showcasing how PMOS and NMOS transistors are strategically employed to realize a spectrum of logic functions, ranging from basic gates like NAND and NOR to more intricate digital circuits. Transitioning into the architectural intricacies of the layout for PMOS and NMOS transistors, the narrative unveils the multi-layered structure required to fabricate these essential components. An overview of these layers, such as the substrate layer, field oxide layer, gate layer, gate oxide layer, source/drain regions, contacts, and metal layer, provides a comprehensive understanding of the construction process. The discussion culminates by underscoring the paramount significance of a standardized skeleton cell, a core entity in CMOS integrated circuit design. This skeleton cell, embodying specific layers, dimensions, and arrangements, serves as a modular and scalable unit in the creation of standardized cells, crucial for realizing intricate integrated circuit architectures. It facilitates efficient power routing solutions, thus playing an indispensable role in achieving optimal functionality and performance in complex integrated circuits.

II. LITERATURE SURVEY

In this Literature survey various works related to Standard cells, their conversion and integration have been reviewed. A. Bahuman; K. Rasheed; B. Bishop [1] discusses a analysis flow for detecting micro latch-up events in ultra-nanometer VLSI technologies. The proposed approach considers the physical layout of the circuit to identify the sensitive points where micro latch-up can occur. A circuit layers mapping tool is developed to analyze the 3D layout geometry and identify potential locations for micro latch-up. Overall, the document presents a comprehensive workflow for analyzing and detecting micro latch-up events in ultra-nanometer VLSI technologies.

A. J. Kessler and A. Ganesan [2] addresses the challenges faced by designers in creating high-tech products with low-cost implementation and short development times. It stresses the need for careful economic trade-offs in VLSI (Very Large-Scale Integration) design, considering integration level, technology choice, packaging, and market timeliness. The standard cell approach is presented as a cost-effective and timely solution, falling between gate arrays and fully custom designs. The tutorial's objective is to guide engineers through the VLSI design process, dispelling the perception that it's exclusively for experts. 4 It covers the entire design process, highlighting potential pitfalls and the importance of design aids. The primary focus is on standard

cell design, with an emphasis on its applicability to both digital and analog circuitry. The article also encourages the development of design aids tailored to standard cell VLSI design.

III. STRUCTURE AND DESIGN OF GRID

Main need of creating the Standard grid cell is repeatability, these standard grid cells are used to design any circuit that follows CMOS logic. The common among all the CMOS logic is PMOS and NMOS transistors. PMOS (P-type metal oxide Semiconductor) and NMOS (N-type metal oxide Semiconductor) transistors play critical roles in CMOS (Complementary Metal-Oxide-Semiconductor) logic design, a fundamental building block of modern integrated circuits. CMOS logic utilizes both types of transistors in a complementary manner to achieve efficient, low-power, and high-performance circuitry. Here's how PMOS and NMOS transistors are used in CMOS logic: Complementary Pairing: CMOS logic leverages the complementary behavior of PMOS and NMOS transistors. PMOS transistors are used to implement the complemented or "true" logic function (e.g., NAND, NOR), while NMOS transistors implement the inverse or "complementary" logic function. Logic Levels: PMOS transistors conduct when the input signal is at logic low (0), i.e., a negative voltage is applied to the gate relative to the source. This conduction allows for the realization of logic high (1) at the output. Conversely, NMOS transistors conduct when the input signal is at logic high (1), allowing for the realization of logic low (0) at the output. Pull-Up and Pull-Down Functionality: In a CMOS inverter, for instance, the PMOS transistor acts as a pull-up device, while the NMOS transistor acts as a pull-down device. When the input (gate) is at logic low, the PMOS transistor conducts, connecting the output to the power supply (VDD), resulting in a logic high output. Conversely, when the input is at logic high, the NMOS transistor conducts, connecting the output to ground (GND), resulting in a logic low output.

Logic Gates: Both PMOS and NMOS transistors are used in various CMOS logic gates, such as NOR gates, NAND gates, and other more complex digital circuits. Depending on the specific logic gate, the PMOS and NMOS transistors will be appropriately arranged to achieve the desired logic function. In the layout of CMOS (Complementary Metal-Oxide-Semiconductor) integrated circuits, both PMOS (P-type Metal-Oxide-Semiconductor) and NMOS (N-type Metal-Oxide-Semiconductor) transistors are typically fabricated using multiple layers to achieve their respective structures. Here's an overview of the common layers involved in the layout for PMOS and NMOS transistors: PMOS Transistor: (1) Substrate Layer (P-Sub): This is the P-type semiconductor layer where the PMOS transistor is built. (2) Field Oxide Layer: Insulating layer used to isolate transistors from each other. (3) Gate Layer: Forms the gate electrode. It's typically made of metal (hence the "metal" in PMOS) or a polycrystalline silicon (polysilicon) material. (4) Gate Oxide Layer: Thin insulating layer between the gate and the channel, ensuring electrical isolation. (5) Source/Drain Regions (P+): Highly doped P-type regions that form the source and drain of the PMOS transistor. (6) Contacts and Metal Layers: These layers facilitate electrical connections to the source, drain, and gate regions. NMOS Transistor: (1) Substrate Layer (N-Sub): This is the N-type semiconductor layer where the NMOS transistor is built. (2) Field Oxide Layer: Insulating layer used to isolate transistors from each other. (3) Gate Layer: Forms the gate electrode. It's typically made of metal or polysilicon. (4) Gate Oxide Layer: Thin insulating layer between the gate and the channel, ensuring electrical isolation. We will first designing the standard grid cell, it is nothing but the skeleton cell of the standard cell, a standard cell can contain many numbers of standard skeleton cells based on the no. of transistor used in the pull up and pull-down network.

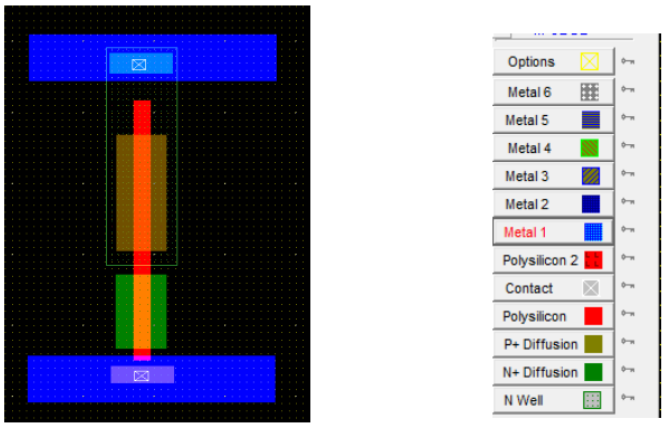
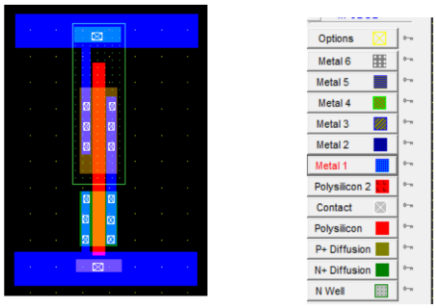


Figure 1 Standard skeleton cell

The height of the standard skeleton cell can be decided by the interconnect space and the width of the NMOS and PMOS. The interconnect space is decided by amount of Metal 2 is needed between the PMOS and NMOS, so it is better to have the height of the standard cell as multiple of metal 2 pitch. The standard skeleton cell consists of the following layer in the layout, (a) *nwell* (b) *n+ diffusion* (c) *p+ diffusion (d) metal 1 for vdd and VSS* (e) *contact* (f) *ploy silicon* And it also offers the routing solution for the power routing problems. When we placed another cell above one cell, the standard will be flipped vertically and place above the current cell array.

A 1X and 2X drive strength inverter has been designed using the standard cell and the nX inverter can be designed using the same skeleton cell and even various gates like flip flops also can be designed just by writing the modelling code like Verilog and extracting the physical design layout for larger digital circuit.



(a)1X inverter

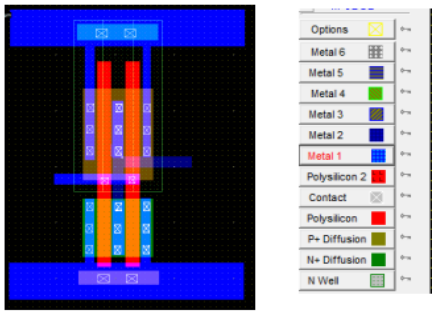


Figure 3 (b) 2X inverter

IV. RESULTS AND DISCUSSION

The skeleton cell could be used very easily the entire digital floorplan, and the accuracy of the skew rate can be achieved same in all the designs using the skeleton cell, so the tuning for skew rate can be avoided mostly in the clock based circuits, the above designs were designed by following the specified Design Rule Checks (DRC), to make sure that devices can be fabricated .

Design rules and electrical parameters

Layer	Width	Spacing	Surface		Surf capa	Lin capa	Dif capa	Res	Thickn	Height	Permitt
	lambda	lambda	lambda2		af/µm2	af/µm	af/µm	ohm	µm	µm	
nitride	0	0	0								
passiv	1330	1330	0								
metal6	8	8	144		100.00		50.00	0.05/sq	0.70	6.60	3.10
via5	5	5	0					1.00/via	0.50	6.10	4.00
metal5	8	8	100		120.00		50.00	0.05/sq	0.70	5.40	3.10
via4	2	4	0					1.00/via	0.50	4.70	4.00
metal4	3	4	16		140.00		50.00	0.06/sq	0.50	4.20	3.10
via3	2	4	0					2.00/via	0.50	3.70	4.00
metal3	3	4	16		160.00		50.00	0.06/sq	0.50	3.20	3.10
via2	2	4	0					2.00/via	0.50	2.70	4.00
metal2	3	4	16		180.00		50.00	0.06/sq	0.50	2.20	3.10
via	2	4	0					2.00/via	0.50	1.70	4.00
metal	3	4	16		200.00		30.00	0.06/sq	0.50	1.20	3.10
poly	2	3	16		400.00			4.00/sq	0.20	0.01	4.00
poly2	2	2	8		400.00			4.00/sq	0.20	0.22	4.00
contact	2	4	0					20.00/via	1.20	0.00	4.00
diffn	4	4	16		350.00	100.00		250.00/sq	0.40	0.00	4.00
diffp	4	4	16		300.00	100.00		300.00/sq	0.40	0.00	4.00
nwell	10	11	144		250.00			120.00/sq	1.00	0.00	4.00
								0.01/sq	0.50	1.00	4.00

Figure 4 Design rules followed in the layout design.

The leakage current will be less as the body biasing comes with skeleton cell so the where the skeleton used the LUP (Latch Up effect) will very less , Simulated current also been attached , using the methods like fingers , the output capacitance will be reduced, so speed can be increased using the standard cells .

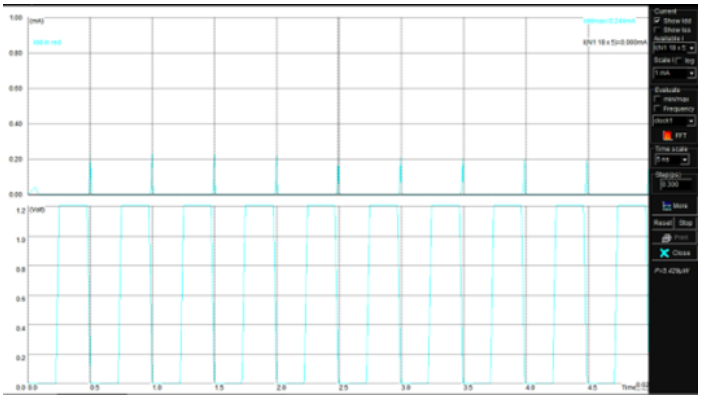


Figure 5 Simulated current.

V. CONCLUSION

The proposed work implements a standard cell of height 36µm PMOS width of 1.5 µm and channel length of 1.5 µm and NMOS width of 1.32 µm. This process can be repeated many times, making it easier to route power grids. The tap connection which is continuous all over the cell offers strong potential at the body terminal which reduces the latch up effect. The standard height of NMOS and PMOS which uses the fingers and multiplier concept offers low rate of electromigration.

VI. REFERENCES

[1]. Y. Yang, J. He and R. Manohar, "Dali: A Gridded Cell Placement Flow," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020, pp. 1-9.

[2]. A. J. Kessler and A. Ganesan, "An introduction to standard-cell VLSI design: Very large scale integration (VLSI) is becoming an important means of producing electronic circuits at low cost, on tight schedules, and with protection for proprietary designs," in IEEE Potentials, vol. 4, no. 3, pp. 33-36, Oct. 1985, doi: 10.1109/MP.1985.6500265.

[3]. A. J. Kessler and A. Ganesan, "Standard cell VLSI design: A tutorial," in IEEE Circuits and Devices Magazine, vol. 1, no. 1, pp. 17-34, Jan. 1985, doi: 10.1109/MCD.1985.6311921. 4. A. E. Dunlop and B. W. Kernighan, "A Procedure for Placement of Standard-Cell VLSI Circuits," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.

[4], no. 1, pp. 92-98, January 1985, doi: 10.1109/TCAD.1985.1270101.

5. A. Bahuman, K. Rasheed and B. Bishop, "An evolutionary approach for VLSI standard cell design," Proceedings of the 2002 Congress on Evolutionary Computation. CEC'02 (Cat. No.02TH8600), Honolulu, HI, USA, 2002, pp. 431-436 vol.1, doi: 10.1109/CEC.2002.1006273.

[6]. S. Azimi and L. Sterpone, "Micro Latch-Up Analysis on Ultra-Nanometer VLSI Technologies: A New Monte Carlo Approach," 2017 IEEE Computer Society Annual Symposium on VLSI

(ISVLSI), Bochum, Germany, 2017, pp. 338-343, doi: 10.1109/ISVLSI.2017.66.

[7]. C. Wu, Y. Tang, Y. Wei and S. Sun, "Generation and Elimination of Antenna Effect," 2021 2nd International Conference on Artificial Intelligence and Computer Engineering (ICAICE), Hangzhou, China, 2021, pp. 836-840, doi: 10.1109/ICAICE54393.2021.00162