A RELIABLE APPROACH FOR THREE STAGE COMPARATOR USING NOR BASED CLOCK GATING TECHNIQUE

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ABSTRACT

This brief presents a reliable approach for a three-stage comparator using a NOR-based clock gating approach, which keeps speed and return noise low while cutting down on power and delay. An additional amplification step in a three-stage comparator boosts both speed and voltage gain. To further boost speed, a three-stage comparator employs nMOS input pairs for both the amplification and regeneration stages. At the amplifier step of the modified three-stage comparator, a CMOS input pair is used. By cancelling out the nMOS kickback through the pMOS kickback, this significantly lowers the kickback noise. In the regeneration step, it also provides an additional signal path, which aids in accelerating the speed even more. The conventional three-stage comparator and its modified version consumes more power due to complexity of the design and switching activity. In this proposed method a NOR based clock gating technique was implemented at the latch stage to reduce the power consumption as well as delay. By employing a clock gating technique using a NOR gate, the comparator disables the clock signal to each stage when not needed, minimizing unnecessary switching activity and reducing power consumption. The NOR gate-based clock gating provides precise control of the clock signal, minimizing leakage current. In comparison to the standard design, the suggested design provides notable reductions in power consumption and latency when implemented in 45 nm technology. The suggested method is effective, as shown by the simulation results, and is therefore appropriate for high-speed and low-power applications. High-performance comparators have a dependable and effective solution in the suggested design.

1. INTRODUCTION

These days, digital processing is used for a lot of applications, including signal processing. Since the analogue to digital converters (ADC) circuit will affect the applications' overall performance, developers of digital integrated circuits (ICs) must create a quick ADC circuit [1]. Processing speed and power consumption are crucial in these applications. A comparator is a component of most ADCs. Therefore, the comparator needs to run quickly and with minimal power. When two analogue signals are compared, a comparator is employed to provide the result in binary signal [2]– [3]. For a comparator, an amplifier circuit is required because its input signals are often low in amplitude. Usually, the starting point of the preamp is an amplifier with differential inputs with active loads. An extremely high gain will be produced by the differential amplifier. The two input voltage differences are amplified by it. The latch or decision-making circuit is linked to the preamplifier's output. By comparing the signals, the decision-making circuit decides which signal is stronger. Preamplifier-based comparators are typically utilized in flash or pipeline ADC architectures [4]. Preamplifier-based comparators use positive feedback and back-to-back latch stages; they are regenerative comparators [5, 6]. The kickback effect is lessened through the preamp in the comparator with latch [1]–[5]. Noise reduction will be aided by this. An inverter's gate capacitance is used as a memory device, and this device is known as a latch [4]. A dynamic latch architecture is frequently employed in analogue circuits due to its exceptional speed and respectable accuracy.

Importance of Low power

Low power design techniques for high-speed applications are crucial, as the market for portable battery-powered gadgets is growing quickly. Voltage scaling is the method used to reduce power. The subthreshold area of operation caused by voltage scaling necessitates the development of novel circuits and architectures to fulfil the rising demands. Process variance has an impact on performance as we step features. Applications such as analogue digital to analogue converters and window comparators use this. In these applications, comparators play a vital role. Comparator design affects the device's overall performance [1]. Comparing particular values to the reference value is an essential function of the comparator.

Importance of comparator in ADC

Over the past few years, analog-to-digital converters, or ADCs, have emerged as a key component propelling the semiconductor industry. ADCs are more conventional and have the ability to provide fast speed with minimal power dissipation due to the increased integration of several functional blocks into a single chip. Furthermore, the semiconductor industry finds ADCs more acceptable because to their small size operations, low power consumption, and decreased propagation latency. Given that high channels drug use, gate-induced

drainage leakage, and group to band tunnelling across the junction are required, scaling down transistor size is not an easy task. It's also necessary to manage the complexity of brief channel effects [1]. Furthermore, due to the tiny size of the transistors, supply voltages must be lowered in analogue circuit design in order to meet the need of reliability [2]. Concerns regarding these aspects are relevant to the comparator, which is the most practical ADC representation.

Latch Based Comparators

For low power and high-speed designs, latch-based comparators are employed. There are two steps in the latch-based comparator. The comparator's preamplifier stage increases the sensitivity of the comparator against noise produced by the feedback stage [2]. The larger input is detected by the latch stage by detecting the slight difference between the inputs. Amplification of the outputs is provided by the output buffer. Comparators' precision is limited by an input reference latch offset voltage that arises from intrinsic load capacitance mismatches, current factor β (= μ COXW/L), and threshold voltage VTH [1]. To attain an effective performance, the planning of these phases is crucial. The double tail comparator, which uses a few extra transistors to reduce delay, is a modification of the traditional comparator for low power and fast operation in [3]. Low power operation sets a limit on the common mode input voltage. In order for different systems to detect small inputs, high-performance comparators must amplify them to a sufficient level [8]. The comparator design suggested in reference [1] employs a fully split with an improved reset architecture that uses gearbox gates to boost speed for sampling and hold less ADC. A quick comparator with excellent precision is an essential component of an ADC [9]. It is preferred to avoid stacking transistor between the rails and instead develop novel circuits for minimal voltage operation, aside from technological changes. Window comparators are employed in systems meant to facilitate evaluation and fault finding. They must also fulfil the low power design requirement. Comparators and an AND gate are used in the traditional windows comparison [4] with volt hysteresis feature, which operates in noisy environments. Many electrical systems depend heavily on comparators, which need to be optimized for maximum performance.

Preamplifier

The input signal is amplified by the preamplifier. For this, the signal is fed into the differential amplifier having active loads that serves as the preamplifier circuit's first stage. A circuit to minimize kickback noise and lessen the impact of offset voltage errors brought on by device mismatch comes next [5]. The circuit used to make decisions connects to the preamplifier's output. By comparing the signals, the decision-making circuit ascertains which signal is stronger. An output buffer circuit subsequently transforms the decision-making circuit's output into a logic signal [2]. To mitigate the impact of offsets voltage error resulting from device mismatch, this preamplifier employs a self-biased split circuit with dynamic loads [8].

Latch

The second level of the comparator system is called a dynamic latch stage. The circuit uses two inverters coupled back-to-back to create a differential comparator. Between the two difference nodes of the latch are likewise employed NMOS transistors. After establishing which input signal is larger, the latch stage will increase the difference between the input signals. The latch will provide a digital output level as its output, representing the positive or negative differential input signal.

Lector Technique

A crucial factor to take into account while designing CMOS VLSI circuits is power dissipation. When it comes to battery-powered applications, high power consumption reduces battery life and has an impact on packaging, cooling costs, and reliability. The primary causes of power dissipation are as follows: 1) leakage current; 2) short-circuit currents resulting from the voltage supply and ground having a conducting path for the brief time required for a logic gate to transition; and 3) capacitive power dissipation caused by the charging and discharge of the load capacitance.

2. LITERATURE REVIEW

Yan Zheng; Fan Ye; Junyan Ren “A 13 bit 100 MS/s SAR ADC With 74.57 dB SNDR in 14-nm CMOS FinFET.” 2020 IEEE International Symposium on Circuits and Systems (ISCAS)**.**

The design and implementation of a 13-bit, 100 MS/s (Mega Samples per second) CMOS FinFET process-fabricated, sequential approximation register (SAR) analog-to-digital converter (ADC) are presented in this work. With a Signal-to-Noise-and-Distortion Ratio (SNDR) of 74.57 dB, the ADC is appropriate for high-speed and high-resolution applications. Because of the smaller transistor size and better electrical properties of 14-nm FinFET technology, there are a lot of benefits in terms of speed and power efficiency. The design incorporates several innovative techniques to enhance performance, including a low-noise reference generator, a high-speed comparator, and an optimized digital-to-analog converter (DAC) architecture.

The paper details the design methodology, circuit implementation, and measurement results. It discusses the challenges of achieving high linearity and low power consumption in advanced process nodes and how these were addressed in the ADC design. Key features of the design include a bootstrapped switch to improve linearity, dynamic element matching in the DAC to reduce nonlinearity errors, and a low-power clocking scheme to minimize power consumption. Measurement results demonstrate the ADC's performance, showing that it achieves a low Total Harmonic Distortion (THD) and a high Spurious-Free Dynamic Range (SFDR), confirming its suitability for high-performance applications in telecommunications and instrumentation.

Ata Khorami; Mohammad Sharifkhani "A Low-Power High-Speed Comparator for Precise Applications" presents a novel comparator design that achieves a remarkable balance between low power consumption and high-speed operation, making it suitable for precise applications. The comparator's design is optimized for low power consumption, operating at a mere 1.2 mW with a supply voltage of 1.2 V, making it ideal for battery-powered devices. Simultaneously, it achieves a propagation delay of just 1.1 ns, enabling high-speed operation that rivals traditional comparators. Furthermore, the comparator exhibits a low input-referred offset of 1.5 mV, ensuring precise decision-making in applications where accuracy is paramount.

The comparator's exceptional performance is achieved through the employment of several innovative design techniques. A differential pair is used to improve noise immunity and reduce input-referred offset, while current-mode logic reduces power consumption and increases speed. Regenerative feedback is also utilized to enhance the comparator's speed and precision. These techniques combine to make the comparator suitable for a wide range of applications, including high-speed analog-to-digital converters (ADCs) in data acquisition systems and image sensors, as well as digital-to-analog converters (DACs) in audio and video processing. Overall, the paper presents a significant contribution to the field of analog circuit design, showcasing a low-power, high-speed comparator design that achieves precise operation, making it an attractive solution for designers seeking to balance power consumption and performance in their applications.

R. Lotfi and S. Babayan-Mashhadi (2014). A Low-Voltage, Low-Power Double-Tail Comparator: Analysis and Design. A 22(2) the IEEE Transactions on Integration of Very Large Scale (VLSI) Systems publication, 343–352.

Dynamic regenerative comparators are becoming more and more popular as a means of achieving the goals of fast speed, low power consumption, and area efficiency in analog-to-digital converters. This research will provide an analysis of the dynamic comparators' latency along with the derivation of analytical expressions. Designers can completely investigate the choices in dynamic comparator design and gain an idea of the primary causes of comparator delay from the analytical expressions. A novel dynamic comparison is proposed, based on the analysis presented. It is a modified version of a traditional double tail comparator circuit designed to operate quickly and efficiently even at low supply voltages. A notable reduction in delay time is achieved by strengthening the favorable reviews during regeneration with minimal transistor additions and without altering the design. The analysis results are validated by post-layout simulation findings in a 0.18-µm CMOS chip. It is demonstrated that there is a significant reduction in both power usage and delay time in the suggested dynamic comparator.

A. Khorami and M. Sharifkhani (2016). Fast and energy-efficient comparator for digital-to-analog conversion. AEU: The International Journal of Communications and Electronics.

For portable electronic devices, low-power, high-speed ADCs make sense as options. Comparators are essential to the effectiveness of widely used ADCs as SAR and Flash ADCs. In the past, static comparators were utilized, but due to their high-power consumption and slow speed, they are not suitable for portable applications. It was suggested to use one-stage dynamic comparators in order to boost speed and decrease power usage. But these comparators have a built-in trade-off between offset voltage and power usage. Additionally, the capacitive link from the comparator's output nodes to its input nodes causes kick-back noise in one-stage dynamic comparators. A two-stage dynamic comparator was suggested as a solution to reduce kickback noise and separate the single-stage dynamic comparator's offset versus speed trade-off. The input transistors within the two-stage dynamic comparisons are selected to be large enough to provide the desired offset voltage. Actually, the first stage nearly entirely determines the comparator's overall offset. Huge parasitic capacitors are created at the first phase of the comparator's output when big transistors are used as the input. As such, there is a trade-off between offset voltage and power consumption. There have been reports of recent techniques to balance voltage or increase speed while consuming less electricity.

SAR ADC Utilizing a Low-Power Speed Comparison for Precise Applications, Neethu Prakash, Society of New Technologies and Creative Studies.

These days, mobile devices are just one of the many applications that depend on low-power, high-speed ADCs. The main components of the various ADC types are comparators. Although they have an extremely high-power consumption due to their constant on state and inherent limited speed, CMOS transistors were employed as static comparators several years ago. The suggested comparator uses a tiny cross-coupled circuit, pMOS latch, and pMOS preamplifier with a unique clocking pattern to modify the preamplifier gain. Since pMOS transistor are utilized as the latch's input and a cross-coupled circuit is used to maintain the preamplifier outputs' common mode voltage at a low level, the clocking pattern offers sufficient preamplifier gain. It is demonstrated that the suggested comparator increases speed while halves power consumption. Additionally, even though pMOS transistor are utilized at the comparator's input, it functions at high input common-mode voltages that are near to VDD. Setting the preamplification delay to its ideal value can also improve comparison speed and cut down on extra power usage. However, this delay is set to a value that is far from its optimal position in the traditional and other comparators. The suggested comparator is therefore a strong contender for accurate power-efficient high-speed applications. The preamplifier's deactivation after the ideal delay greatly lowers the power usage. As a result, it increases speed and uses less electricity. A latch and preamp with inputs nMOS transistors can be constructed utilizing the suggested structure in place of nMOS transistors. Because nMOS transistors are inherently better than pMOS ones, this will lead to a faster speed. An SAR ADC can be created with this comparator. Cadence is the instrument being utilized.

In summary, this approach improves speed.

Hollman, J., and Lu, J. (2013). A low-power High-Precision Comparator with Time-Domain Bulk-Tuned Bias Cancel. Seminars on Circuits and Systems, IEEE

To lower the input-referred offset of a low-power, high-precision dynamic comparator with the least amount of additional power and delay, an innovative time-domain bulk-tuned offsets cancellation method is used. With a broad range of common mode input, the offset cancellation approach can achieve quick and robust convergence without introducing noticeable offset or noise. The comparator and OC circuitry together use less energy while operating at a 5 V supply and 200 kHz clock frequency.

3. EXISTING METHOD

Low-power, high-speed ADCs are required for digitally wireless communication applications like Ultra-Wide-Band (UWB) and Wired Personal Area Network (WPAN networks) in order to transform radio frequency and intermediary frequencies into digital form for baseband computation. ADC uses comparators extensively, making them significant devices [1]. In numerous applications such as switching power regulators, data transfer, ADCs, and others, comparators are employed. A key component of high-speed ADCs is the comparator architecture. The two most important parameters in comparator design are power consumption and speed [2]. Regardless of design, the comparator is a fundamental component of all high-speed ADCs and plays a major role in determining the general efficiency of data converters. Bit resolution, total power consumption, and the highest sampling rate are all included.

Perhaps the most underappreciated and underused monolithic linear component is the comparator. This is sad since comparators are among the most adaptable and widely used parts out there. The IC op amp's dominance in analogue design can be attributed, in large part, to its adaptability. In many cases, comparator devices are thought of as 1-bit A/D converters, which are rudimentary digital expressions of analogue signals. This is a valid point of view, in theory. Additionally, its outlook is wastefully restrictive. Similar to how op amps do more than "just amplify," comparators do more than "just compare." Linear circuit functions as complex as an op amp-based circuit can be implemented with comparators, especially high-speed comparators. High performance outcomes can be obtained by carefully matching an op amp with a quick comparator. Op-amp-based circuits typically take use of their precise feedback loop closure. Such loops are best maintained constantly over an extended period of time. Comparator circuits, on the other hand, frequently operate depending on speed and produce an output that is discontinuous across time. Although each method has advantages, the best circuits are produced by combining the two.

demonstrates the three-stage comparator used in this project. One follows the other as all three stages are connected. One more preamp (the second stage) has been added as compared to the Miyahara comparator, which is the main distinction. By acting as an inverter, the additional preamp allows the latch stage to use the nMOS output pair M11–12 rather than the pMOS input pair, increasing speed. In addition to providing voltage gain, the additional amplifier also reduces noise and input referred offset while speeding up regeneration. While the additional preamplifier aids in speeding up the process, this extra step adds to

the delay because the boosted signal must pass through two stages instead of one before reaching the latch stage. Therefore, it is imperative to deliberate whether the additional delay outweighs the benefits it confers. Its outputs, FP and FN, fall to GND following the first-stage amplification, as shown in Fig. As a result, the enormous gate-source voltage of the second-stage output pair M8–9 is identical to VDD. Because of this, M8–9 has enough current to rapidly pull up RP and RN. This indicates that in comparison to the latch stage's significant delay (about 200 ps in post-layout simulation), the additional delay caused by the second stage is little (around 20 ps). This makes sense because the second stage is essentially a low-delay dynamic inverter. Moreover, the first-stage output load in the three-stage comparator is only M8–9 in Fig., in contrast to the first-stage output load in the Miyahara's comparator (M6-7 and M12–15 in Fig.). The amplification speed is increased by many times when the output load is decreased.

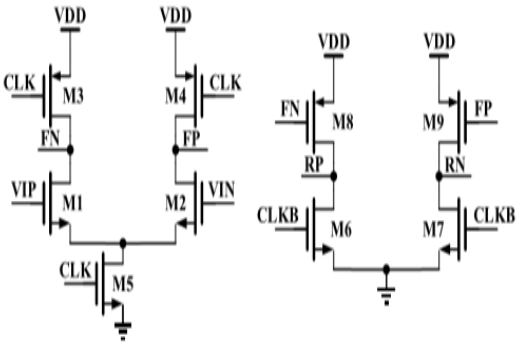

Figure 1 (a) First two stages (preamplifiers).

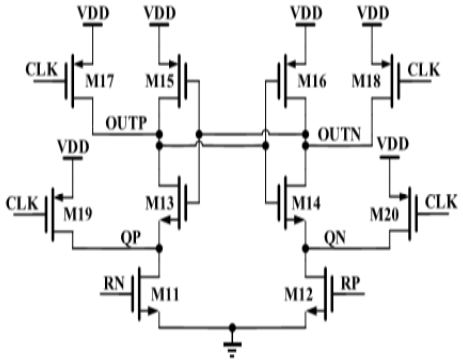

Figure 1 (b) Third stage (latch stage)

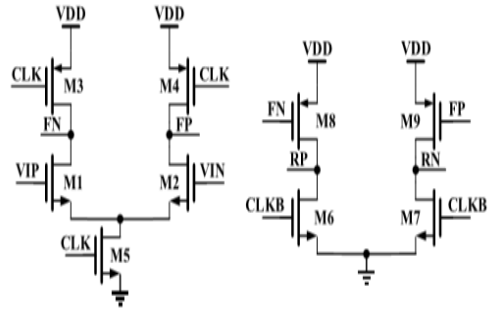

Figure 2 (a) Original first two stages (preamplifiers) with nMOS input pair.

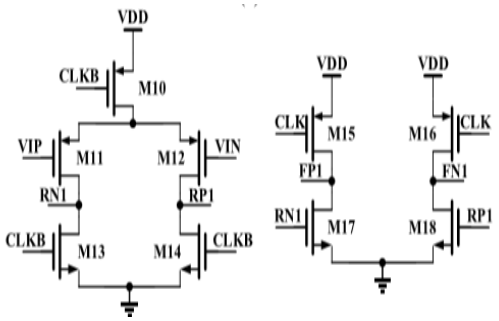

Figure 2 (b) Extra first two stages (preamplifiers) with pMOS input pair.

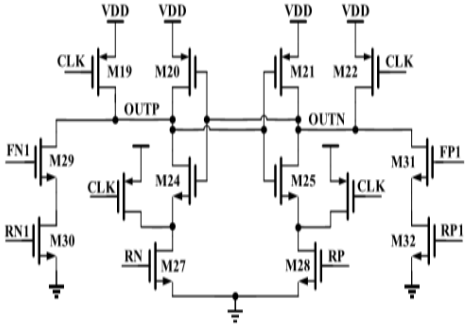

Figure 2 (c) Third stage (latch stage).

As can be seen in, this brief recommends modifying the three-stage comparator to further boost speed and reduce kickback noise. The only way the updated version varies from the one used in the previous section is that it has two extra stages and extra routes M's 29–32 in the latching stage of the additional initial two levels make advantage of two pMOS inputs.

M11–12 removes the return noise of the nMOS output pair M1-2. The extra routes M29–32, which additionally apply additional signal to the latching nodes OUTP and OUTN, speed up regeneration even more while suppressing noise and reference offset in the inputs. The following describes how these extra circuits work. During the reset phase, CLKB is 1 and CLK is 0. In Figure 4(b), the reset values of RP1 and RN1 are set to GND, and FP1 and FN1 to VDD. Consequently, the additional path M29–32 (Fig. 4(c)) has no static power. Moreover, this turns off M30 and M32.

CLK rises to 1 and CLKB falls to 0 during the amp phase. In Fig. 4(b), where R stands for rising, RP1 & RN1 ascend to VDD, after which FP1 and FN1 fall to GND (fall is denoted by the letter F). Since the increasing value of RP1 and RN1 occurs after the decreasing of FP1 and FN1, the additional pathways in Fig. 4(c) are temporarily enabled, pulling an offset present to the latching node OUTP and OUTN. This accelerates the regeneration phase that follows and reduces noise and the comparator output referred offset by generating a different voltage at OUTP or OUTN. the other paths in Figure 4(c) were once more flipped, and the FP1 so that FN1 fell to GND.

"Three-stage comparators may consume more power compared to simpler designs. More complex designs inherently consume more power due to increased component count, active circuitry, and continuous operation requirements of additional features."

4. PROPOSED METHOD

Introduction

This chapter covers the three-stage comparison plus its modified version that makes use of the clock gating technique. We present the clock gating approach, a novel leakage power reduction method utilizing NOR logic gates. The third stage of operation in three-stage comparators is the latch-based comparator that we are employing in this instance. Two extra tail transistors in a latch-based comparator are inserted which are controlled by NOR based clock, this helps in reducing power consumption.

Clock Gating Technique.

By reducing power or delay depending on the circuit, the clock gating approach reduces circuit requirements by requiring an additional logic to provide a clock enabling signal. This signal is only enabled when the circuit design dictates that it should be logic 0 or 1.

Gate based clock gating

One of the most straightforward methods is gate-based clock gating, which has an easy-to-implement design. Any gate can be utilized with this method. The AND, OR, and NOR gates are the ones that are being discussed. By employing a clock gating technique using a NOR gate, the comparator disables the clock signal to each stage when not needed, minimizing unnecessary switching activity and reducing power consumption. The NOR gate-based clock gating provides precise control of the clock signal, minimizing leakage current.

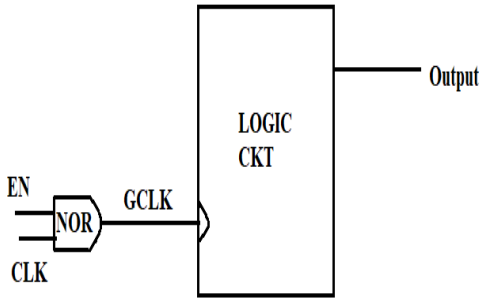

Figure 3 Model diagram of clock gating technique

Schematic of NOR Gate using GDI Logic

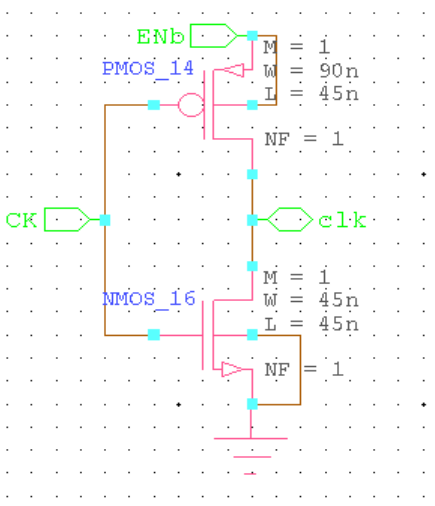

Figure 4 Schematic of NOR gate using GDI Logic

Three stage comparators

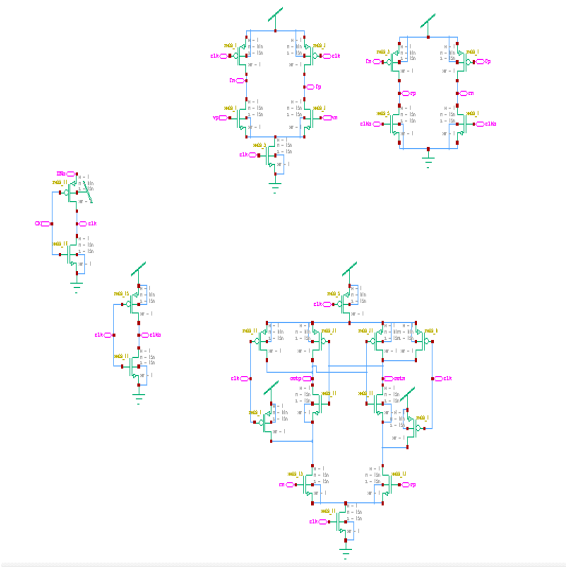

Figure 5 Schematic of proposed three stage comparators

A three-stage comparator consists of the latch stage, the first two stages of which function as preamplifiers. In the third stage, the clock gating approach is used to sketch the design. This method allows us to lower both the circuit's latency and power usage.

Modified Three stage Comparator:

The modified version contains extra pathways in the latch stage and extra stages for the first two, that is the only difference between it and the initial version in the preceding section.

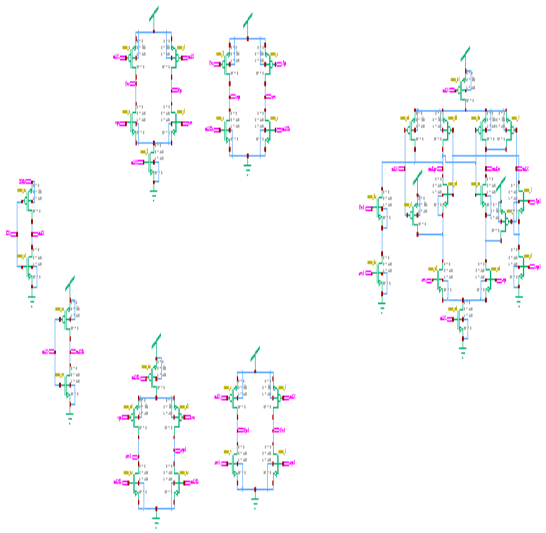

Figure 6 Schematic of proposed modified version of three stage comparator

Less power consumption, reduced output reference offset and noise, reduced kickback noise, and faster speed are all benefits of the redesigned three-stage comparator. For SAR ADCs with high resolution and speed, it is appropriate. For instance, our time-interleaved noise-shaping SAR ADC can benefit from the suggested updated version.

Advantages

1. Reduced dynamic power consumption due to NOR based clock gating technique, Clock signal is only enabled when necessary.
2. Minimized switching activity in the comparator stages which is suitable for battery-powered devices and energy-efficient applications.
3. Enhanced speed performance compared to traditional comparators which is suitable for high-speed applications such as data acquisition systems and image sensors
4. Decreased delay time due to optimized stage design and clock gating technique which will improve the timing performance and accuracy.

Applications

There are several applications of Comparator

- Devices that employ audio and video make use of them.
- They're utilized in mobile phones.
- In image sensors with CMOS technology for mobile applications, they are commonly used.
- They are employed in medical imaging and medical instrumentation.

5. RESULTS

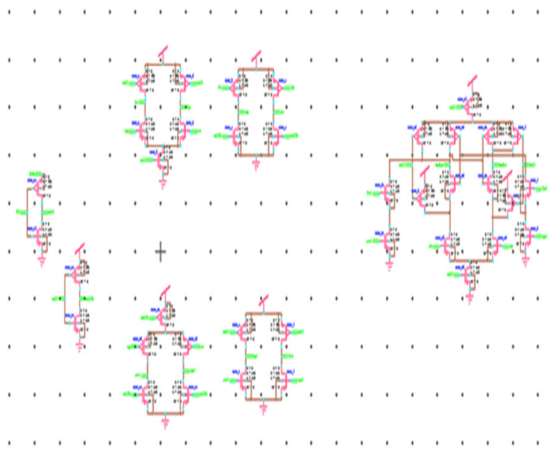

Figure 7 Schematic diagram proposed modified comparator

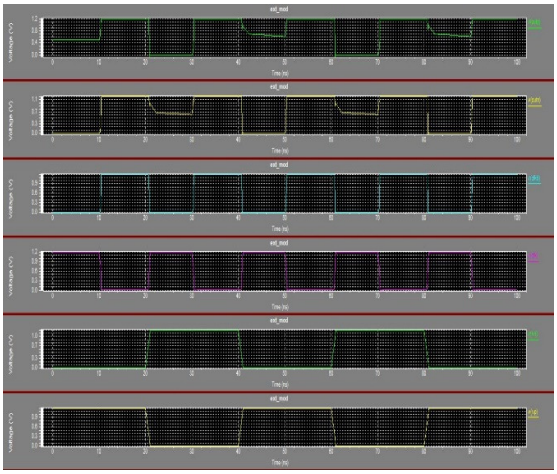

Figure 8 Waveform of proposed comparator

Table:1 Evaluation of power, delay, area parameters

	Three stage comparator (TSC) (Existing)	Modified version of TSC (Existing)	Three stage comparator (Proposed)	Modified version of TSC (Proposed)
Area	19	32	25	38
Delay (ns)	0.63	0.40	0.20	0.19
Power (uW)	3.1	5.4	1.7	2.9

CONCLUSION

The three-stage comparison & its revised version, which has the benefits of high speed and minimal kickback noise, are presented in this brief. The suggested work uses a clock gating method at a latch-based comparator to reduce power consumption. High-speed, high-resolution SAR ADCs are an excellent fit for these comparators. The efficacy of these comparators is finally confirmed by measured outcomes. In 45 nm technology, Tanner EDA is used to implement every design.

REFERENCES

1. Babayan-Mashhadi, S., & Lotfi, R. (2014). Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator. IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 22(2), 343–352.
2. Khorami, A., &Sharifkhani, M. (2016). High-speed low-power comparator for analog to digital converters. AEU - International Journal of Electronics and Communications.
3. Neethu Prakash, SAR ADC Using Low Power High Speed Comparator for Precise Applications, journal of Emerging Technologies and Innovative Research.
4. M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, “A low noise self-calibrating dynamic comparator for high-speed ADCs,” in Proc. IEEE Asian Solid-State Circuits.
5. Lu, J., &Holleman, J. (2013). A Low-Power High-Precision Comparator with Time-Domain Bulk-Tuned Offset Cancellation. IEEE Transactions on Circuits and Systems.
6. Ata Khorami, Mohammad Sharifkhani, Excess power elimination in high-resolution dynamic comparators, Microelectronics Journal, Volume 64,2017, Pages 45-52, ISSN 0026-2692.
7. Amaya, A., Villamizar, R., & Roa, E. (2016). An offset reduction technique for dynamic voltage comparators. 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics
8. Shilpi Singh, A novel cmos dynamic latch comparator for low power and high speed, International Journal of Microelectronics Engineering (IJME), Vol. 1, No.1, 2015
9. Yan Zheng;Fan Ye;Junyan Ren “A 13 bit 100 MS/s SAR ADC With 74.57 dB SNDR in 14-nm CMOS FinFET.” 2020 IEEE International Symposium on Circuits and Systems (ISCAS).
10. Athanasios T. Ramkaj; Michiel S. J. Steyaert; Filip Tavernier “A 13.5-Gb/s 5-mV-Sensitivity 26.8-ps-CLK–OUT Delay Triple-Latch Feedforward Dynamic Comparator in 28-nm CMOS.” 2019 IEEE Solid-State Circuits Letters.
11. Ata Khorami; Mohammad Sharifkhani “A Low-Power High-Speed Comparator for Precise Applications” 2018 IEEE Transactions on Very Large-Scale Integration (VLSI) Systems.
12. Mehdi Nasrollahpour; Chi-Hsien Yen; Sotoudeh Hamedi-hagh “A High-Speed, Low-Offset and Low-Power Differential Comparator for Analog to Digital Converters.” 2017 International SoC Design Conference (ISOCC).
13. Ata Khorami; Mahmood Baraani Dastjerdi; Ali Fotowat Ahmadi “A Low-power High-speed Comparator for Analog To Digital Converters.” 2016 IEEE International Symposium on Circuits and Systems (ISCAS).
14. Satyabrata Nanda; Avipsa S. Panda “Design of Conventional three-stage CMOS comparator in 90-nm CMOS Technology and comparative analysis with its counterparts.” 2015 International Conference on Smart Sensors and Systems (IC-SSS).