SAPON-Based Offset Cancelling Tri-State Sensing Latch: Enhancing Precision and Power Efficiency in NAND Flash Memory

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Abstract: NAND flash memory density increases, the demand for high-precision, low-power sensing latches intensifies. The offset cancelling sensing latch (OCSL) has been a promising solution, but suffers from issues such as energy consumption and data corruption risk due to short-circuits between VDD and GND during operation. To address these challenges, this paper proposes the offset cancelling tri-state sensing latch (OCTSL). The OCTSL enhances read precision and reduces energy consumption by introducing several innovations. Firstly, it employs a tri-state sensing latch to eliminate VDD-GND short-circuits during the sense phase. Secondly, it integrates a sensing node precharge mechanism to prevent short-circuits during the sample phase. Additionally, a couple-down phase leveraging a coupling capacitor enables the use of the tri-state latch without compromising precision or power efficiency. Comparative analysis with the OCSL demonstrates that the OCTSL effectively minimizes variations in effective trip voltages, significantly lowers energy consumption during sample and sense phases, and eliminates the risk of data corruption. Moreover, the use of SAPON (stackly arranged low power ON transistor) technology further enhances performance by reducing power consumption and delays, albeit with a minor increase in die area.This study demonstrates the efficacy of OCTSL in advancing NAND flash memory technology towards higher performance and reliability in read operations.

***Key Words*—**CMOS analog integrated circuits, flash memories, latches, low-noise sense amplifiers, offset canceling.

1. INTRODUCTION

The "High-Precision and Low-Power Offset Canceling Tri-State Sensing Latch" in NAND Flash Memory refers to a design approach to enhance the accuracy and efficiency of reading data from NAND flash memory cells High-Precision: The design aims to achieve precise reading of stored data by implementing an offset canceling mechanism. This involves compensating for any offset or error in the trip voltage, reducing variations and improving the accuracy of the read operation. Low-Power: The design prioritizes energy efficiency by minimizing power consumption during the sensing and sampling phases of the read operation. This is crucial for improving the overall power efficiency of NAND flash memory, especially as memory density increases. Tri-State Sensing Latch: The use of a tri-state sensing latch in the design helps eliminate short-circuits between the power supply (VDD) and ground (GND) during the sense phase. This contributes to reducing energy consumption and enhancing the precision of the read operation. This approach focuses on achieving high precision in reading NAND flash memory while keeping power consumption low. It employs an offset canceling technique and incorporates a tri-state sensing latch to address the challenges associated with accuracy and energy efficiency in NAND flash memory systems.

The page buffer is a crucial circuit that powers the cell string and reads stored data by sensing a bit-line current (IBL) determined by the threshold voltage of the selected cell. In a conventional page buffer's read operation, four phases include bit-line precharge, sensing node precharge, develop, and sense, involving actions such as connecting the bit-line, clamping with a bit-line clamp, and converting threshold voltage data. To prevent errors from coupling between bit-lines, the sensing node precharge phase charges the sensing node capacitor to VDD. In the conventional page buffer, the sensing latch minimizes transistor count for efficient data storage but faces variations in intrinsic trip voltage (VTRIP). The conventional sensing latch, used in NAND flash memory, faces challenges such as VTRIP variation leading to imprecise sensing, especially with numerous page buffers. As word-line numbers increase and multi-level cell technology advances, the sensing latch size decreases, exacerbating VTH.CELL distribution issues. The proposed Offset Canceling Tri-State Sensing Latch (OCTSL) addresses these concerns by introducing features like a tri-state sensing latch in the sense phase to minimize VTRIP variation, a sample phase with sensing node precharge to reduce energy consumption and prevent data corruption, and a couple-down phase using a sensing node coupling capacitor to facilitate tri-state sensing latch adoption, ensuring high precision and low power.

2. LITERATURE REVIEW

Kim, Jin-Ki & Sakui, Koji & Lee, Sung-Soo & Itoh, Yasuo & Kwon, Suk-Chon & Kanazawa, K. & Lee, Ki-Jun & Nakamura, Hiroshi & Kim, Kang-Young & Himeno, Toshihiko & Kim, Jang-Rae & Kanda, Kazushige & Jung, Tae-Sung & Oshima, Yoichi & Suh, Kang-Deog & Hashimoto, Kazuhiko & Ahn, Sung-Tae & Miyamoto, Junichi. (1997).
A 120-mm2 64-Mb NAND flash memory achieving 180 ns/Byte effective program speed. Solid-State Circuits,

IEEE Journal of. 32. 670 - 680. 10.1109/4.568831.
Emerging application areas of mass storage flash memories require low cost, high density flash memories with enhanced device performance. This paper describes a 64 Mb NAND flash memory having improved read and program performances. A 40 MB/s read throughput is achieved by improving the page sensing time and employing the full-chip burst read capability. A 2-μs random access time is obtained by using a precharged capacitive decoupling sensing scheme with a staggered row decoder scheme. The full-chip burst read capability is realized by introducing a new array architecture. A narrow incremental step pulse programming scheme achieves a 5 MB/s program throughput corresponding to 180 ns/Byte effective program speed. The chip has been fabricated using a 0.4-μm single-metal CMOS process resulting in a die size of 120 mm² and an effective cell size of 1.1 μm².

J. H. An, J. Y. Chun, H. K. Park and S. -O. Jung, "All-Bit-Line Read Scheme With Locking Bit-Line and Amplifying Sense Node in NAND Flash," in IEEE Access, vol. 9, pp. 28001-28011, 2021, doi: 10.1109/ACCESS.2021.3058391.
A NAND flash memory senses a cell current in the range of tens of nA, which is smaller than other nonvolatile memories in the read operation. Because of the small cell current, it is difficult to improve the latency and accuracy of the read operation. The improvement of read latency has been a major challenge for the all-bit-line (ABL) sensing architecture because the BL coupling capacitance caused by the off cell limits the BL pre-charge time. In this paper, a high-speed BL pre-charge scheme with an off-cell-like BL locking (OCBLL) is proposed to reduce the BL coupling capacitance between the off-cell BL and the adjacent BL. The deviation of the latch trip voltage caused by the variations in process, voltage, and temperature (PVT) presents another challenge because the deviation increases the read error owing to the small cell current. A sense-out-node amplification (SOA) scheme is proposed to amplify the voltage of the sense-out-node according to the cell current. The SOA scheme generates a large voltage difference despite the small cell current difference. In the simulation with HSPICE models under the same BL-to-BL coupling ratio, it is found that the proposed schemes improve the speed of the BL pre-charge operation by 75% and reduce the read error by 57%.

R. -A. Cernea et al., "A 34 MB/s MLC Write Throughput 16 Gb NAND With All Bit Line Architecture on 56 nm Technology," in IEEE Journal of Solid-State Circuits, vol. 44, no. 1, pp. 186-194, Jan. 2009, doi: 10.1109/JSSC.2008.2007152.
A 16 Gb 4-state MLC NAND flash memory augments the sustained program throughput to 34 MB/s by fully exercising all the available cells along a selected word line and by using additional performance enhancement modes. The same chip operating as an 8 Gb SLC device guarantees over 60 MB/s programming throughput. The newly introduced All Bit Line (ABL) architecture has multiple advantages when higher performance is targeted and it was made possible by adopting the “current sensing” (as opposed to the mainstream “voltage sensing”) technique. The general chip architecture is presented in contrast to a state of the art conventional circuit and a double size data buffer is found to be necessary for the maximum parallelism attained. Further conceptual changes designed to counterbalance the area increase are presented, hierarchical column architecture being of foremost importance. Optimization of other circuits, such as the charge pump, is another example. Fast data access rate is essential, and ways of boosting it are described, including a new redundancy scheme. ABL contribution to energy saving is also acknowledged.

3. EXISTING METHOD

3.1 OFFSET CANCELING SENSING LATCH

Offset Canceling Sensing Latch likely refers to a circuit or mechanism designed to mitigate or cancel out offset errors in sensing applications. In sensing circuits, offsets can lead to inaccuracies. The offset canceling sensing latch is likely designed to suppress or eliminate these offsets, ensuring more accurate and reliable sensing measurements. This technology is commonly used in various electronic systems, especially in applications where precise and offset-free sensing is critical, such as in instrumentation, sensors, or analog-to-digital converters The Offset Canceling Sensing Latch (OCSL) is a technology designed to address significant variations in VTRIP (threshold voltage reference) in NAND flash memory. It incorporates an offset canceling NMOS and a coupling capacitor (CSN.CPL). During the read operation, it utilizes sample and couple-up phases instead of sensing node precharge. In the sample phase, the offset canceling NMOS samples VTRIP, and in the couple-up phase, the sensing node coupling (SNC) node is boosted by CSN.CPL.

Efficient control of the SNC node using GND and VDD, along with CSN.CPL, offers a cost-effective solution for specific design nodes. The OCSL enhances VTRIP accuracy by adjusting the starting voltage (VSN.START) based on the sampled VTRIP, ensuring precise reading of VTH.CELL data with reduced VTRIP.EFF variation. Despite its advantages, the Offset Canceling Sensing Latch (OCSL) encounters challenges. These include elevated energy consumption during the sense phase due to momentary VDD-GND connection, increased energy usage from additional short-circuits in the sample phase, and a potential risk of corrupting sensing latch data. The short-circuit in the sample phase induces a voltage drop in the Latch_S node, diminishing

the static noise margin and posing reliability concerns, potentially leading to the flipping of sensing latch data.

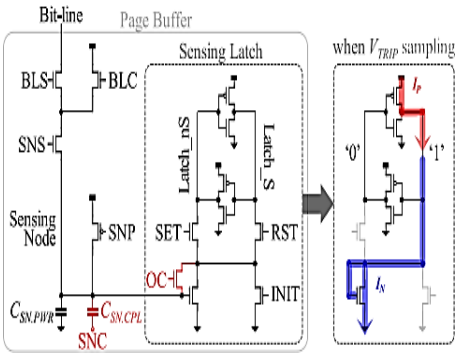

Figure1 Page buffer and read operation of OCSL

4. PROPOSED METHOD

The Offset Canceling Tri-State Sensing Latch (OCTSL) improves upon the Offset Canceling Sensing Latch (OCSL) by introducing three key features. Firstly, it incorporates a tristate sensing latch during the sense phase, eliminating short-circuits between VDD and GND and reducing variation in the threshold voltage (VTRIP). The shielding of floating nodes enhances noise insensitivity. Secondly, in the sample phase, OCTSL includes sensing node precharge, reducing energy consumption and eliminating the risk of corrupting latch data. During the read operation, VTRIP is sampled by connecting a precharged sensing node to the discharge NMOS, minimizing energy use. Lastly, OCTSL includes a couple-down phase with a sensing node coupling capacitor, enabling tristate latch adoption and lowering the sensing node voltage for precise readings. A new DC regulator is introduced with minimal die area overhead to control the sensing node discharge level during the couple-down phase. Overall, OCTSL addresses short-circuit issues, VTRIP variation, and energy consumption, providing a more robust and efficient sensing latch design.

The Offset Canceling Tri-State Sensing Latch (OCTSL) is an improved version addressing issues in the Offset Canceling Sensing Latch (OCSL). It introduces three key features to enhance performance.Tri-State Sensing Latch: In the sense phase, OCTSL incorporates a tri-state sensing latch, which helps eliminate short-circuits between power (VDD) and ground (GND). This reduces variation in the threshold voltage (VTRIP) and enhances overall stability. Additionally, the floating nodes (Latch_S and Latch_nS) are shielded to improve noise immunity. Sensing Node Precharge in Sample Phase: During the sample phase, OCTSL includes sensing node precharge, which not only reduces energy consumption but also eliminates the risk of corrupting latch data. The read operation involves sampling VTRIP by connecting a precharged sensing node to the discharge NMOS, minimizing energy usage. Couple-Down Phase with Sensing Node Coupling Capacitor: OCTSL incorporates a couple-down phase with a sensing node coupling capacitor. This enables the adoption of a tri-state latch, lowering the sensing node voltage for more precise readings. A new DC regulator is introduced with minimal die area overhead to control the discharge level of the sensing node during the couple-down phase, ensuring accurate and efficient operation.

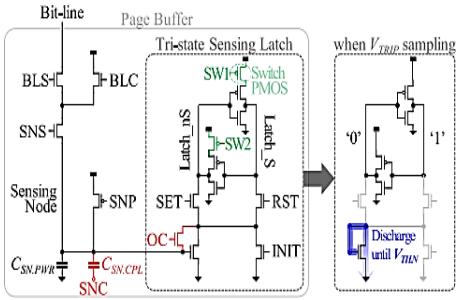

Figure 2 Page buffer and read operation of OCTSL

5. TANNER TOOL

5.1 SIMULATION TOOL

The design cycle for the development of electronic circuits includes an important pre-fabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to efficient design. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication. Tanner EDA tool is a complete circuit design and analysis system that includes:

a) **Schematic Editor (S-Edit):** Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations. S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. Its efficient design capture process integrates easily with third-party tools. S-Edit enables you to explore design choices and provides an easy-to-use view into the consequences of those choices. A faster design cycle gives you more flexibility in moving to an optimal solution—freeing up more time and resources for process corner validation. The results are less risk downstream, higher yield, and quicker time to market.

b) **T-Spice Circuit Simulator:** T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits. The simulator includes the latest and best device models available, as well as

coupled line models and support for userdefined device models via tables or C functions. T-Spice uses an extended version of the SPICE input language that is compatible with all industry standard SPICE simulation programs. All of SPICE's device models are incorporated, as well as resistors, capacitors, inductors, mutual inductors, single and coupled transmission lines, current sources, voltage sources, controlled sources, and a full complement of the latest advanced semiconductor device models from Berkeley and Philips Labs.

c) **Waveform Editor (W-Edit):** W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation. Visualizing the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding, and improving those circuits. W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.

6. RESULTS

Schematic diagram: -

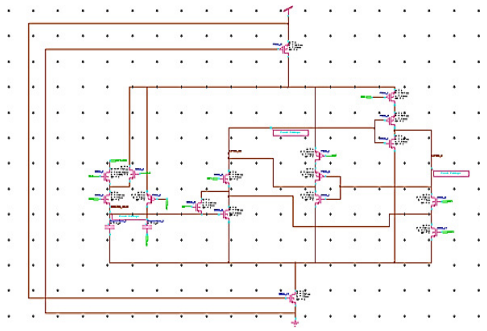

Figure 3 Schematic diagram of OCTSL using SAPON technique

Simulation results: -

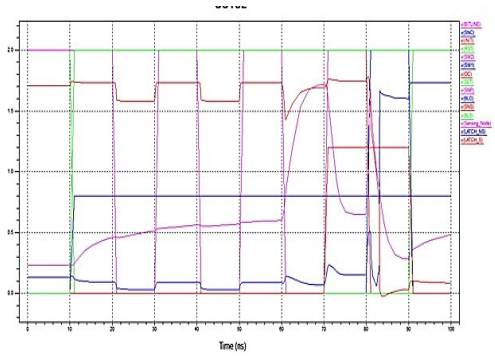

Figure 4 Waveform of OCTSL with SAPON technique

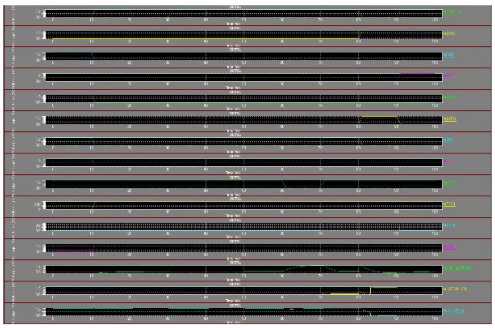

Figure 5 Detailed and expanded waveform of OCTSL with SAPON technique

Area results: -

```
*  Device and node counts:
*              MOSFETs - 17                MOSFET geometries - 4
*                  BJTs - 0                          JFETs - 0
*              MESFETs - 0                         Diodes - 0
*            Capacitors - 2                      Resistors - 0
*             Inductors - 0                  Mutual inductors - 0
*  Transmission lines - 0          Coupled transmission lines - 0
*     Voltage sources - 13                 Current sources - 0
*                  VCVS - 0                          VCCS - 0
*                  CCVS - 0                          CCCS - 0
*    V-control switch - 0                 I-control switch - 0
*       Macro devices - 0          External C model instances - 0
*          HDL devices - 0
*          Subcircuits - 0               Subcircuit instances - 0
*   Independent nodes - 77                    Boundary nodes - 14
*          Total nodes - 91
```

Power results: -

```
* BEGIN NON-GRAPHICAL DATA

Power Results
v1 from time 0 to 1e-007
Average power consumed -> 8.980757e-004 watts
Max power 1.511798e-003 at time 6.1e-008
Min power 4.354233e-004 at time 8.06823e-008


* END NON-GRAPHICAL DATA
```

Delay results:

```
* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay = 7.3101e-008
   Trigger = 1.0050e-008
   Target  = 8.3151e-008

* END NON-GRAPHICAL DATA
```

Comparison table: -

	Area	Power	Delay
Existing	15	1.31088e-003W	7.1492e-007nS
Proposed	17	8.980757e-004W	7.3101e-008nS

CONCLUSION

Through the integration of the tristate sensing latch with the Offset Canceling Sensing Latch (OCSL), significant changes occur in the sense phase, rendering it independent from the inverter PMOS. This modification notably eliminates the inherent voltage variation in the trip point caused by the inverter PMOS. Additionally, incorporating the tristate sensing latch eliminates short-circuit currents during read operations, leading to a substantial decrease in energy consumption during both sample and sense phases. Furthermore, the absence of short-circuit currents in read operations mitigates the risk of data corruption in the sensing latch during the sample phase. Overall, this enhancement in the sensing latch mechanism enhances stability, reduces energy consumption, and improves data integrity during the sample phase, thus contributing to a reduction in power consumption and delay through the SAPON Approach.

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