"Design of 8-bit 12T SRAM with Multi-Node Upset Recoverability

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***Abstract*—With the advancement of technology, the size of transistors and the distance between them are reducing rapidly. Therefore, the critical charge of sensitive nodes is reducing, making SRAM cells more vulnerable to soft-errors. If a radiation particle strikes a sensitive node of the standard 6T SRAM cell, the stored data in the cell are flipped, causing a single-event upset (SEU). Therefore, in this project, a Design of 12T SRAM With Multi-Node Upset Recoverability is proposed to mitigate SEUs. 12T SRAM cell can recover from the effect of single-event multi-node upsets (SEMNUs) induced at its storage node pair. Along with these advantages, the proposed cell exhibits the highest read stability, as the '0'-storing storage node, which is directly accessed by the bitline during read operation, can recover from any upset. 12T SRAM cell also exhibits higher write ability and shorter write delay than most of the comparison cells. All these improvements in the proposed cell are obtained with respect to recently published soft-error-aware SRAM cells 12T SRAM Cell is designed using Cadence Virtuoso tool in 45 nm technology. The proposed cell also exhibits less Read and Write Access time compared to previously proposed QUCCE12T, QUATRO12T, less Read and Write access time compared to QUATRO12T, 11.11% and 55.5% less Read and Write access time compared to RHPD12T and 12.7% less and 22% more Read and Write access time compared to QUCCE12T.**

***Index Terms*—12T-SRAM, Single-Event Upset(SEU), Multi-Node Upset(MNU), Cadence, 45 nm, Read/Write Delay.**

I. Introduction

Microprocessors are widely used with multiple cores to upgrade their performance. A larger number of cores implies that a higher amount of cache memory is required. Hence, SRAM cells, which are used as cache memory, play a vital role in the power, area, and delay optimization of the processor. SRAM or Static Random Access Memory is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of computer memory gains its name from the fact that data is held in the memory chip in a static fashion. The data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear. SRAM has the advantage that it offers better performance than DRAM because DRAM needs to be refreshed periodically when in use, while SRAM does not. However, SRAM is more expensive and less dense than DRAM, so SRAM sizes are orders of magnitude lower than DRAM.

Radiation particles impact the functionality of memory circuits. On striking the substrate of an integrated circuit, such as semiconductor memory, an energetic particle generates electron-hole pairs. The electric field resulting from the reverse bias between the diffusion region and substrate/n-well is perceived by the strike-generated minority carriers as a forward field [1]. Consequently, minority carriers drift towards the drain diffusion regions, and upon accumulation, a voltage spike, either positive or negative, is generated depending on the type of minority carrier. If the magnitude of the spike surpasses the switching threshold of the logic circuit and persists for a sufficient duration, the stored data may flip, leading to a phenomenon known as a SEU orsoft-error [2].

Moreover, as the spacing between devices on an integrated circuit decreases significantly due to aggressive technology scaling, a strike by a single ion may impact multiple nodes, potentially resulting in a SEMNU. To counteract the impact of SEUs on memory, Triple Modular Redundancy (TMR) has been employed [3]. This approach involves utilizing three replicas of memory cells, with the majority voting mechanism determining the correct output. In case one copy experiences a flip, the other two will dominate the voting process, ensuring the correct output [4]. However, this technique imposes substantial area and power overheads, rendering it impractical for many designs.

An alternative method to mitigate the impact of SEUs is through the use of Error Correction Codes (ECCs) [5]. However, ECCs increases significant power, area, and delay overheads as they require redundancy and additional devices for encoding and decoding circuits. Consequently, soft-error-aware SRAMs are favoured over ECCs due to their lower power, area, and delay consumption. Additionally, it is desirable for SRAM cells to possess multi-node upset recovery capability in addition to SEU recovery ability [9]. Due to the positive feedback of cross-coupled inverters in the 6T SRAM cell results in an SEU at one storage node automatically altering the content of the other storage node. Consequently, the 6T cell does not possess the characteristics expected of a Soft-Error-Aware SRAM.

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Consequently, the 6T cell does not possess the characteristics expected of a Soft-Error-Aware SRAM [10].

To address the above-mentioned issues, we introduce a new type of memory cell called the 12T SRAM With Multi-Node Upset Recoverability [1]. Figure 1 shows complete design of 12T SRAM Cell, which is immune to SEUs of both polarities induced at any sensitive node. The proposed cell can recover from SEMNUs that occur at its storage node-pair. 12T SRAM Cell shows enhanced read stability as the '0'-storing storage node, which is directly accessed by the bitline during read operation, can recover from any upset. The proposed cell shows higher write ability and shorter write delay than most of the comparison cells.

II. Methodology

An introduction about the basic operations and SEU recovery ability of the proposed 12T SRAM cell is given. The schematic of the 12T SRAM Cell is illustrated in Figure 1. The structure consists of two wordlines, WL and WWL, controlling various transistors within the cell. Additionally, it includes two storage nodes, Q and QB, along with two internal nodes, S1 and S0.

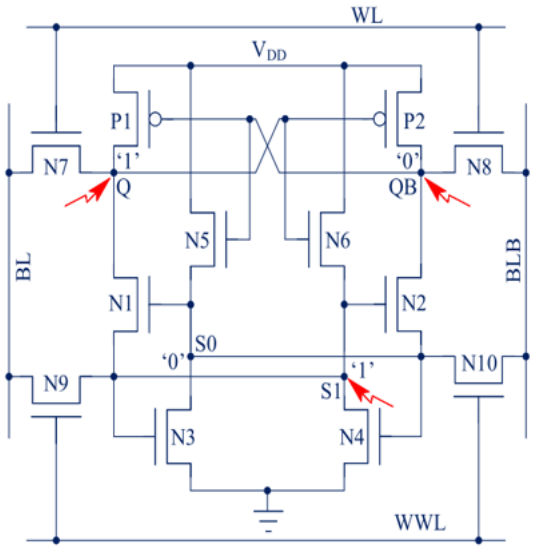

Fig. 1. Schematic of the proposed 12T SRAM cell

A. Basic Operations

All the basic operations of the proposed 12TSRAM cell are mentioned in this sub-section.

1) Hold Operation: During the hold mode, the access transistors in both pairs are deactivated by pulling down both WL and WWL to the ground (GND). To minimize read delay, the bitlines are precharged to the power supply voltage (VDD) during hold mode. Consequently, while the cell is in the hold state, transistors P1, N2, N3, and N6 remain activated (ON), while the remaining transistors remain deactivated (OFF) for the scenario under consideration. As a result, the 12T SRAM cell retains its initially stored data.

2) Write Operation: During the write operation, both wordlines (WL and WWL) are activated, causing both pairs of access transistors (N7/N8 and N9/N10) to turn ON. To change the stored data (i.e., writing '0' at Q), BL is connected to the ground (GND), while BLB is clamped at the power supply voltage (VDD). As BL is connected to GND, nodes Q and S1 are pulled down by BL through N7 and N9, respectively. Consequently, node Q activates transistor P2 and deactivates transistor N6, while node S1 deactivates transistors N2 and N3. Meanwhile, nodes QB and S0 are pulled up by BLB through N8 and N10, respectively. Consequently, node QB deactivates transistor P1 and activates transistor N5, while node S0 activates transistors N1 and N4. The interaction between transistors P1 and P2 amplifies the potential difference between Q and QB. Similarly, the interaction between transistors N3 and N4 enhances the potential difference between S1 and S0. As a result, the write operation is executed successfully.

3) Read Operation: During the read operation, WL is connected to the power supply voltage (VDD), while WWL remains deactivated. As a result, access transistors N7 and N8 are activated, allowing access to the storage nodes. Conversely, the other access transistors (N9 and N10) remain deactivated. For reading, the bitlines are precharged to VDD. Consequently, BLB discharges through N8, N2, and N3. Meanwhile, since N1 and N4 are deactivated, BL remains at VDD. This setup is depicted in Figure 2. Once the voltage difference between BL and BLB reaches 50 mV, a sense amplifier can detect the stored data, thus completing the read operation.

B. SEU Recovery Analysis

This subsection provides a concise overview of the proposed cell's behaviour when its sensitive nodes experience a SEU. A sensitive node refers to the vicinity of the reverse biased drain diffusion region of an OFF transistor. When a radiation particle strikes the drain terminal of a PMOS transistor, it generates a transient pulse, either '0' to '1' or '1' to '1', depending on the initial data stored in the node. Conversely, if an energetic particle hits an NMOS transistor, it produces a transient pulse, either '0' to '0' or '1' to '0'. It's important to note that in the 12T SRAM cell, the '0'-storing internal node (S0) is surrounded only by drain terminals of NMOS transistors. Consequently, only a '0' to '0' transient pulse is generated, which doesn't alter the logic state of the node. 12T SRAM Cell shows enhanced read stability [18] as the '0'-storing storage node, which is directly accessed by the bitline during read operation, can recover from any upset. Therefore, for the '1'-storing case of 12T SRAM (where Q = '1', QB = '0', S1 = '1', and S0 = '0'), node S0 is not sensitive, while the other nodes (Q, QB, and S1) are sensitive to SEUs.

1) SEU @ S1: When the '1'-storing internal node S1 is affected by a SEU, causing its value to change from '1' to '0' as shown in Figure 2, transistors N2 and N3 are deactivated. However, the pull-up transistor P2, associated with QB, remains deactivated due to the unaffected node Q. Consequently, both the pull-up and pull-down paths related to QB are disconnected, causing node QB to enter a high

impedance state. Typically, a high impedance state doesn't alter the logic state of the node. Therefore, QB maintains its initial logic value and keeps transistor N5 deactivated. As a result, node S0 also enters a high impedance state (as both N5 and N3 are deactivated) and preserves its initial logic value. Since nodes Q, QB, and S0 retain their states, S1 is able to recover its original state.

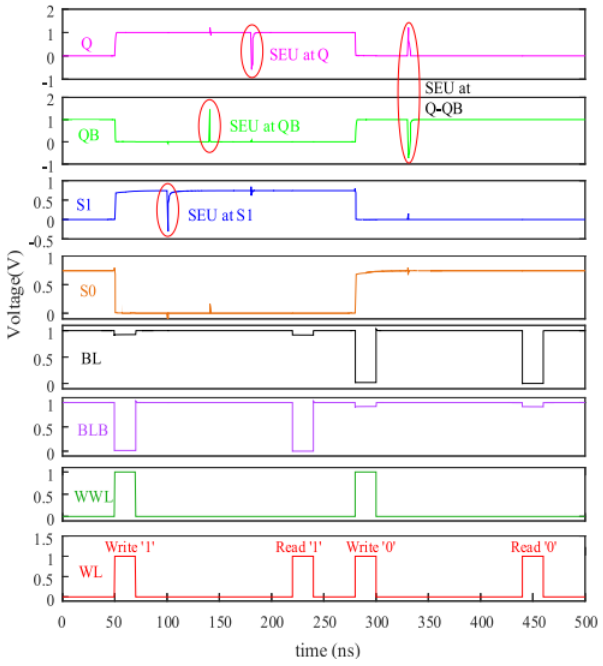

Fig. 2. Basic operation and SEU recovery at different nodes

2) SEU @ Q: When the '1'-storing storage node Q is affected by a SEU, causing its logic state to transition to '0', transistors P2 and N6 are momentarily activated and deactivated, respectively. With N6 turned off and N4 remaining off (due to hold mode), node S1 enters a high impedance state and preserves its logic value. Consequently, N2 and N3 remain activated. Although P2 is activated, since the NMOS transistors N2 (2.5×) and N3 (2.5×) are made larger than the PMOS transistor P2 (1×), QB maintains its original logic level. Since QB retains its state, P1 remains activated and N5 remains deactivated. Additionally, with N3 being activated, S0 remains at '0' and keeps N1 deactivated. Therefore, Q successfully restores its original data, as depicted in Figure 2.

3) SEU @ QB: When a SEU with sufficient strength affects the '0'-storing storage node QB, its logic value changes to '1'. Consequently, P1 is temporarily deactivated, and N5 is temporarily activated. However, despite N5 being activated, node S0 maintains its logic state because N3 (which remains activated due to hold mode) is made larger (2.5×) than N5. Therefore, both N1 and N4 remain deactivated. As both the pull-up (P1) and pull-down (N1) transistors corresponding to Q are deactivated, node Q enters a high impedance state and preserves its initial logic state. Since N4 remains deactivated and N6 (driven by Q) remains activated, S1 maintains its original logic value, thereby keeping N2 and N3 activated. Consequently, node QB is discharged to the ground (GND).

4) SEU @ Q-QB: When both storage nodes Q and QB are simultaneously affected by a SENMU, node Q transitions from '1' to '0', while node QB changes from '0' to '1'. Consequently, Q activates transistor P2 and deactivates transistor N6. Similarly, QB deactivates transistor P1 and activates transistor N5. Despite N5 being activated, node S0 maintains its logic level, as explained in Section II-B.3. Since S0's logic state remains unaffected, transistors N1 and N4 remain deactivated. As both N6 and N4 are deactivated, node S1 enters a high impedance state and retains its original logic state. Therefore, N2 and N3 remain activated, causing QB to discharge to ground (GND). Since N1 is deactivated (due to S0 retaining its state) and P1 is activated (driven by QB), node Q returns to '1'. Consequently, both Q and QB recover their original states.

12T SRAM cell exhibits the capability to recover from the impact of a SEU occurring at node S1, Q, or QB, as well as from a SENMU affecting the Q-QB node-pair. However, there remains a possibility of data alteration if sufficient charge accumulates at the S1-Q/S1-QB node-pair. In such a scenario, node S1 may transition from '1' to '0', deactivating transistors N2 and N3, while node Q/QB may change from '1' to '0'/'0' to '1', deactivating N6/P1 and activating P2/N5.

III. Experimental Results

The performance characteristics of the newly proposed 12T SRAM cell have been evaluated using 45-nanometer CMOS technology. To facilitate comparison, the estimated performance metrics of the 12T SRAM are contrasted with those of other modern cells, namely QUCCE12T, QUATRO12T, RHD12T. The dimensions specified in the respective research papers are adopted for the simulation of QUCCE12T, QUATRO12T, and RHD12T to ensure a fair comparison of their performance against the 12T SRAM cell.

A. Basic Operations of 12T SRAM cell

The transient waveform of a 12T SRAM cell as shown in Figure 3 typically refers to the voltage or current behavior over time during different operations such as read, write, or standby modes.

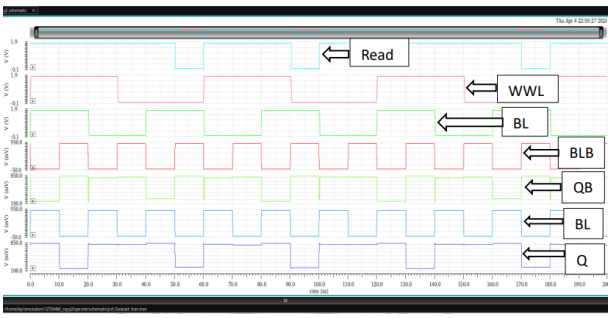

Fig. 3. Basic Operations of 12T SRAM cell

During a read operation as shown in Figure 3, the wordline is activated, enabling access to the storage nodes. As the stored data is read out, the bitline voltages change based on the logic values stored in the cell. During a write operation, the write waveform illustrates the voltage or current changes as new data is written into the cell. When initiating a write operation, the wordline and appropriate bitline(s) are activated to select the target cell for writing. Voltage or current pulses are applied to the selected bitlines to write the desired data into the storage nodes.

B. Single-Event-Upset Recoverability

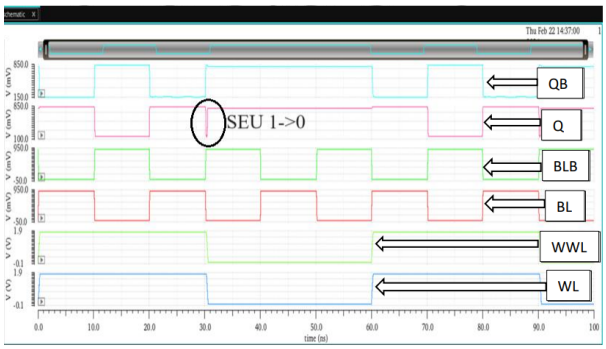

Fig. 4. Single-Event-Upset Recoverability Waveform

A sensitive node is the surroundings of the reverse biased drain diffusion region of an OFF transistor. If a radiation particle strikes the drain terminal of a PMOS, it produces either a '0'→'1' or '1'→'1' transient pulse, based on the data that the node was storing initially. On the other hand, if an energetic particle strikes an NMOS, it generates either a '0'→'0' or '1'→'0' transient pulse as shown in Figure 4.

C. Read and Write Access time

Write-access time represents the time duration from the point when WL is activated to that of the time where the storage node reaches to 90% of VDD value for writing the logic. The read access time for SRAM refers to the amount of time it takes for the memory to return the data stored at a particular address after a read request is made. This time is measured from when the address is presented to the SRAM to when the data is available on the data output lines.

Read and Write Access time of the newly proposed 12T SRAM cell have been evaluated using 45-nanometer CMOS technology. To facilitate comparison, the estimated performance metrics of the 12T SRAM are contrasted with those of other cells, namely QUCCE12T, QUATRO12T, RHD12T given in Table I. The dimensions specified in the respective research papers are adopted for the simulation of QUCCE12T, QUATRO12T, and RHD12T to ensure a fair comparison of their performance against the 12T SRAM cell. Figure 4.5 and Figure 4.6 shows the comparison graph of Read/Write access time of 12T SRAM Cell with existing design.

TABLE I
COMPARISON OF READ AND WRITE ACCESS TIME

Designs	Read Access Time	Write Access Time
RHD12T [6]	70 ps	28 ps
QUCCE12T [7]	55 ps	22 ps
QUATRO12T [8]	90 ps	20 ps
Proposed 12T SRAM	63 ps	18ps

D. 8-bit Transient waveform of 12T SRAM cell

An 8-bit waveform of a 12T SRAM cell shown in Figure 5 illustrate the behavior of the SRAM cell during read or write operations involving 8 bits of data. For a write operation, the waveform would similarly illustrate the behavior of the bitlines and the application of voltage or current pulses to write 8 bits of data into the SRAM cell. Generating such waveforms involves circuit simulations using tools such as Cadence Virtuoso.

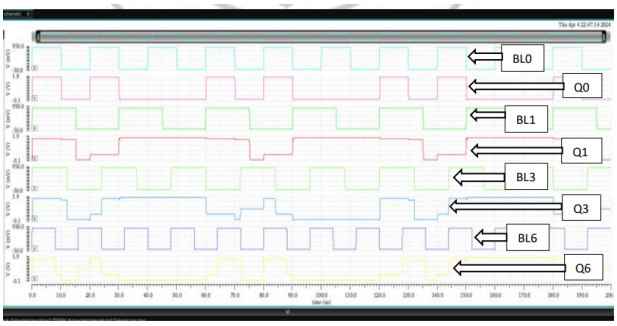

Fig. 5. 8-bit Transient waveform

These simulations model the behavior of the 12T SRAM cell under various conditions and provide detailed waveforms for analysis and optimization.

E. Area Comparison

Layouts of all the considered cells are drawn to compare the area of 12T SRAM with that of other cells. The area of all the considered cells, with respect to 12T SRAM, is reported in Table II. It can be observed from the table that 12T SRAM Cell consumes slightly larger area than the 12T cells, QUCCE12T and QUATRO12T. This is due to the use of larger pull-down transistors in the proposed cell. Even though RHD12T also has 12 transistors in its design, it occupies a larger area than 12T SRAM Cell because it has more PMOS in its cell design compared to the proposed 12T SRAM Cell. It iss observed that the 12T SRAM cell occupies a slightly larger area than QUCCE12T and QUATRO12T due to the utilization of larger pull-down transistors. It can be observed from Table II that 12T SRAM Cell consumes slightly larger area than the 12T cells, QUCCE12T and QUATRO12T. This is due to the use of larger pull-down transistors in the proposed cell.

IV. CONCLUSION

This project presents a novel design for an 8-bit 12T SRAM, focusing on addressing the challenges posed by radiation-

TABLE II
AREA COMPARISON

Designs	Area (um2)
RHD12T [6]	1.99
QUCCE12T [7]	1.61
QUATRO12T [8]	1.55
Proposed 12T SRAM	1.82

induced upsets. The 12T SRAM configuration is carefully crafted to ensure the preservation of original data integrity, particularly at sensitive nodes, which are susceptible to alteration due to radiation strikes. Additionally, the SRAM design showcases the capability to recover from multi-node upsets originating from a single ion strike targeting the storage node-pair. This recovery feature enhances the reliability and resilience of the SRAM, making it suitable for deployment in radiation-prone environments where data integrity is paramount. In addition to these advantages, the proposed cell significantly reduced read and write access times compared to previously introduced designs such as QUCCE12T, QUATRO12T, and RHD12T. The 12T SRAM cell demonstrates a notable improvement, with 42.8% and 11.11% less read and write access time respectively compared to QUATRO12T. Moreover, it exhibits 11.11% and 55.5% less read and write access time respectively compared to RHD12T. In comparison to QUCCE12T, the proposed cell showcases a 12.7% decrease in read access time and a 22% increase in write access time, highlighting its competitive performance in terms of access speeds. The Layout of 12T SRAM Cell is designed and area of 12T SRAM Cell is 1.82 um2. Area of 12T SRAM Cell is compared to previously proposed QUCCE12T, QUATRO12T and RHD12T. Proposed 12T SRAM cell has 14.8% more area compared to QUATRO12T, 9.34% less area compared to RHD12T and 11.5% more area compared to QUCCE12T. 12T SRAM Cell has slightly more area compared to QUCCE12T and QUATRO12T.

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