DESIGN AND IMPLEMENTATION OF FUZZY CONTROL OF FLYBACK MULTI-OUTPUT SOFT SWITCHING CONVERTER USING DIGITAL SIGNAL PROCESSOR

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Abstract: *The current trend is to opt for high-frequency operation of power converters, as the allowable size and weight of power converters for aerospace power systems is highly restricted to accommodate greater payload. As the hard switched converters suffered from drawbacks of high frequency switching, soft switched quasi-resonant converter is designed in this paper. Also to overcome the drawbacks of frequency modulation control which requires wide band of frequency range, a new control technique which combines the advantages of inductor freewheeling and frequency modulation is proposed to operate wide range of load. In digital systems, the power supply voltages have been reduced considerably in recent years and often digital components requiring different voltages are present in the same board. Hence in this work by considering all the above mentioned factors, a intelligent control of flyback multi-output zero voltage switching quasi-resonant converter is developed and presented using TMS320F2407A DSP. The proposed converter is suitable for aerospace applications.*

Keywords: **We would like to encourage you to list your keywords in this section**

1. INTRODUCTION

Switched Mode Power Supplies (SMPS) are widely used in applications such as computers, aerospace systems and communication equipments. Since dc-dc converters form the central part of the SMPS, small size and reduced weight can be achieved by operating the converter switches at high switching frequency. In addition, the dynamic characteristics of the converter will also improve at high operating frequencies. By designing proper control to the converter, dc output voltage at desired level can be obtained. DC-DC converters can be classified as hard-switched and soft-switched converters. It is important to design converter circuits capable of operating at high frequencies owing to the ever-increasing demand of high-power density switched mode converters in aerospace applications. At high frequencies hard-switched converters are unsuitable because of high switching losses, switching stresses, reduced reliability, electro-magnetic interference (EMI) and acoustic noise [1]. Switching losses can almost be eliminated in soft-switched converters, as the switching operations of the device are possible when the voltage across or current flow through the switch, is equal to zero value.

This work mainly focuses on design, analysis and control of quasi-resonant converters(QRCs), which are obtained by introducing LC resonant circuits near the PWM switch. By this method the device current or device voltage is forced to oscillate in a quasi-sinusoidal manner to create either zero current switching (ZCS) or zero voltage switching (ZVS) conditions.

Multi-output dc-dc converters, which provide several, regulated and isolated outputs are widely used in the above-mentioned applications. It is often better to add an additional secondary winding to the transformer, each with its own rectifier and output filter instead of providing a separate supply for each output. Many literatures have reported the analysis and design of multi-output hard-switched dc-dc converters. However, the hard-switched converters used for this purpose will be less efficient while operating at high frequencies. The control of multi-output constant frequency CF-ZVS-QRCs have been reported by implementing analog controller[3][4].

The flyback topology operating in continuous conduction mode (CCM) is very attractive for low power applications like broadband access devices due to low parts count and good cross regulation of multiple outputs. In the proposed topology, the resonant components are placed on the primary side of the isolation transformer when compared to other topologies. This in turn reduces the number of resonant components required for achieving ZVS thereby reducing the weight of the converter. However, the power level of the multi-output flyback ZVS-QRC is limited to low power applications.

Due to complex nonlinear behavior of the QRCs, which makes difficult to derive the small-signal model of the converters, which in turn further complicates the conventional controller design. For this reason, the present work focuses mainly on the design and implementation of intelligent control techniques for QRCs. The voltage regulation of QRCs can be achieved either by using frequency modulation(FM) or constant frequency(CF) techniques. Reference[5] presents the simulation of intelligent control of flyback multi-output ZVS QRC. Hence, in this work, it is proposed to design and develop conventional fuzzy logic controller(CFLC) for the voltage control of multi-output flyback ZVS-QRCs using TMS320F2407A DSP.

2. ANALYSIS AND DESIGN OF MULTI-OUTPUT FLYBACK ZERO VOLTAGE SWITCHING QUASI-RESONANT CONVERTER

The flyback topology operating in continuous conduction mode (CCM) is very attractive for lower power applications like broadband access devices due to low parts count and good cross regulation of multiple outputs. The circuit diagram of multi-output flyback ZVS-QRC is shown in the fig.1. The switch S_1 is the main switch. The elements L_r and C_r form the series resonant tank circuit. The resonant components L_r and C_r are placed in the primary side of the isolation transformer. Both switches S_1 and S_2 operate under zero voltage condition. By adding an auxiliary switch S_2 in parallel with the resonant inductor L_r, the switching frequency band required to regulate the output voltage for a given load change is reduced. The auxiliary switch S_2 is used to control the OFF time of the switching period. The transformer serves to step down/up the input voltage, reverses the output

voltage polarity and provides the energy storing during the operation. The circuit produces two voltages V_{o1} and V_{o2}. Here, the converter is operated in half-wave mode. The elements L_m, L_1 and L_2 represent the primary, secondary1 and secondary2 inductances respectively. The current through the primary of the transformer is assumed as i_{Lm}.

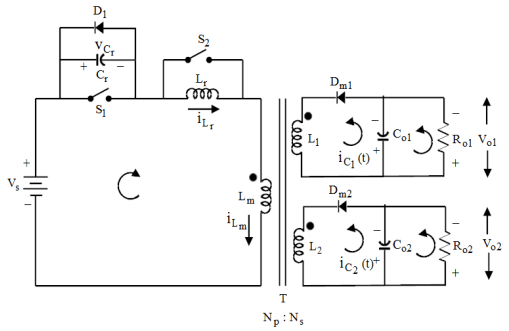

Fig. 1. Circuit Diagram of multi-output flyback ZVS-QRC.

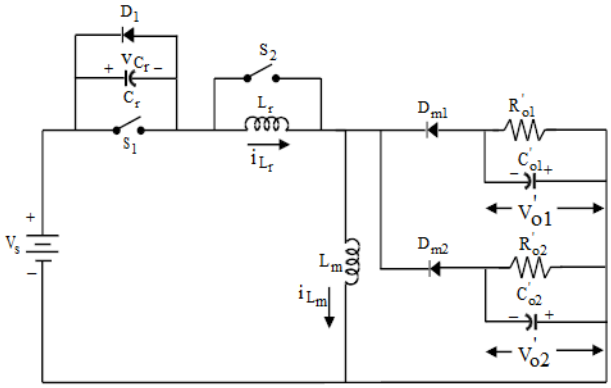

Fig. 2. Equivalent circuit with components in the secondary side of the transformer referred to primary.

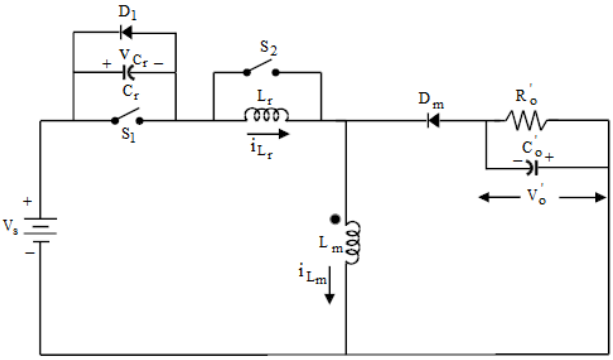

Fig. 3. Modified circuit with secondary side of the transformer referred to the primary side with single output.

To analyze the converter steady-state behaviour[1], the following assumptions are made:

1. Magnetizing inductance (L_m) is larger than resonating inductance (L_r).
2. The magnetizing inductance L_m with output filter capacitances (C_{o1}, C_{o2}) and the load resistances R_{o1}, R_{o2} are treated as constant sinks of current I_{o1} and I_{o2}.
3. The output filter capacitances (C_{o1}, C_{o2}) along with the loads R_{o1}, R_{o2} are treated as constant sinks of voltage V_{o1} and V_{o2}.
4. Semiconductor switches are ideal, i.e. no forward voltage drops in the ON-state, no leakage currents in the OFF-state and no time delays at both turn-ON and turn-OFF.
5. Reactive elements in the circuit are ideal.
6. Transformer windings are tightly coupled without leakage inductances. To further simplify the analysis, the components in the secondary side are transferred to the primary side by neglecting the effect of leakage inductances as shown in fig. 2.The turns ratio is defined as

$$n_k = \frac{N_k}{N_p} \quad ; k=1,2$$

where N_p - number of turns in primary, N_1 - number of turns in secondary1 and N_2 - number of turns in secondary2. The output voltages V_{o1} and V_{o2} can be referred to the primary as V'_{o1} and V'_{o2} and they are denoted as

$$V'_{ok} = \frac{V_{ok}}{n_k} = V'_o \quad ; k = 1, 2. \qquad \text{(Referring fig. 2)}$$

To analyze the steady state operation of ZVS-QRC, it is divided into six stages [4]. For analysis, the state variables are taken as i_{L_r} and v_{C_r}. The equivalent circuit for each stage is shown in fig.4. The theoretical resonant waveforms are shown in fig.5.The following circuit parameters are defined for analysis:

i. Characteristics impedance $Z_o = \sqrt{\frac{L_r}{C_r}}$ (1)

ii. Resonant angular frequency $\omega_o = \frac{1}{\sqrt{L_r C_r}}$ (2)

iii. Resonant frequency $f_o = \frac{1}{2\pi\sqrt{L_r C_r}}$ (3)

iv. Normalized load resistance $R = \frac{R_o}{Z_o}$ (4)

iv. Normalized switching frequency $f_{ns} = \frac{f_s}{f_o}$ (5)

2.1. Linear Capacitor Charging Stage ($t_0 \leq t < t_1$)

The switch S_1 is opened (OFF) to begin a new cycle at $t=t_0$ and freewheeling diode D_m is OFF. The equivalent circuit diagram for this stage is shown in fig. 4(a). During this stage, the maximum primary current I_M flows through the resonant capacitor C_r and its voltage increases linearly from zero to $(V_s+V_o^{'})$. The capacitor voltage v_{C_r} is governed by the equation,

$$v_{C_r(t)} = \frac{I_M t}{C_r} \quad (6)$$

When the resonant capacitor voltage $v_{C_r}(t)$ reaches $(V_s+V_o^{'})$ at $t = t_1$, the diode D_m gets forward biased. The duration of this stage T_{d1} is given by

$$T_{d1} = t_1 - t_o = \frac{C_r(V_s+V_o^{'})}{I_M} \quad (7)$$

In fig.5, the resonant capacitor voltage and resonant inductor voltage V_{C_r} and V_{L_r} denotes the drain to source voltage of S_1 and S_2, respectively. Similarly V_{g1} and V_{g2} denote the gating pulse to switch S_1 and S_2, respectively. The voltage waveform of the resonant capacitor contains both $DC(V_s+V_o^{'})$ and $AC(I_M Z_o)$ components. The AC component should be more than the DC component as there is a lower bound on the load current, below which the ZVS property will be lost. For fixed V_s, the increase in load current increases the peak value of the capacitor voltage causing a high voltage stress across the switch.

2.2. Resonant Inductor Discharging Stage ($t_1 \leq t < t_2$)

Stage 2 begins at $t = t_1$. Since $v_{c_r} > V_o^{'}$, the diode D_m becomes forward biased. The elements L_r and C_r form a series resonant circuit. The equivalent circuit diagram of this stage is shown in fig.4(b).The state equations are

$$C_r \frac{dv_{C_r}}{dt} = i_{L_r}(t) \quad (8)$$

$$L_r \frac{di_{L_r}}{dt} = (V_s+V_o^{'}) - v_{C_r}(t) \quad (9)$$

With initial conditions $v_{C_r}(t_1) = V_s+V_o^{'}$ and $i_{L_r}(t_1) = I_M$, the solutions of the above state equations are

$$v_{C_r}(t) = (V_s+V_o^{'}) + I_M Z_o \sin\omega_o t \quad (10)$$

$$i_{L_r}(t) = I_M \cos\omega_o t \quad (11)$$

$$v_{L_r}(t) = -I_M Z_o \sin\omega_o t \quad (12)$$

At $t=t_1^{'}$, i_{L_r} reaches zero value and v_{C_r} reaches its peak value as shown in fig.5 and it is given by,

$$v_{C_r}(t') = v_{C_{r,peak}} = (V_s + V_o') + I_M Z_o \quad (13)$$

The current I_M should be sufficiently large so that

$$I_M Z_o > (V_s + V_0')$$

is satisfied to obtain the ZVS condition. Otherwise, the switch S_1 voltage will not come back to zero naturally, resulting in turn-ON loss. At $t = t_2$, i_{L_r} and v_{C_r} reaches $-I_M$ and $(V_s + V_o')$, respectively. When v_{L_r} reaches zero at $t = t_2$, the switch S_2 is turned ON as shown in fig.5. The duration of this stage is T_{d2} which is equal to $t = t_2$.

$$T_{d2} = t_2 - t_1 = \frac{\pi}{\omega_o} \quad (14)$$

2.3. Holding Stage ($t_2 \leq t < t_3$)

This is the new stage, which characterizes the multi-output flyback ZVS-QRC. The constant switching frequency operation is achieved by introducing the holding stage during which i_{L_r} and v_{C_r} are held constant. The voltage v_{L_r} is clamped at zero value by keeping the switch S_2 closed. The equivalent circuit diagram of this stage is shown in fig.4(c). The resonant capacitor and inductor current are given by,

$$v_{C_r}(t) = V_s + V_o' \quad (15)$$

$$i_{L_r}(t) = -I_M \quad (16)$$

This stage continues until S_2 is turned OFF at $t = t_3$. The duration of this stage is T_{d3} which is equal to $t_3 - t_2$.

2.4. Resonant Inductor Charging Stage ($t_3 \leq t < t_4$)

Resonance of L_r and C_r resumes in this stage as shown in fig.4(d),when S_2 is turned OFF at $t = t_3$ and the corresponding state equations are

$$L_r \frac{di_{L_r}}{dt} = (V_s + V_0') - v_{C_r}(t) \quad (17)$$

and

$$C_r \frac{dv_{C_r}}{dt} = i_{L_r}(t) \quad (18)$$

with initial conditions $v_{C_r}(t_3) = (V_s + V_o')$ and $i_{L_r}(t_3) = -I_M$. The solutions of the above equations (17) and (18) are given by

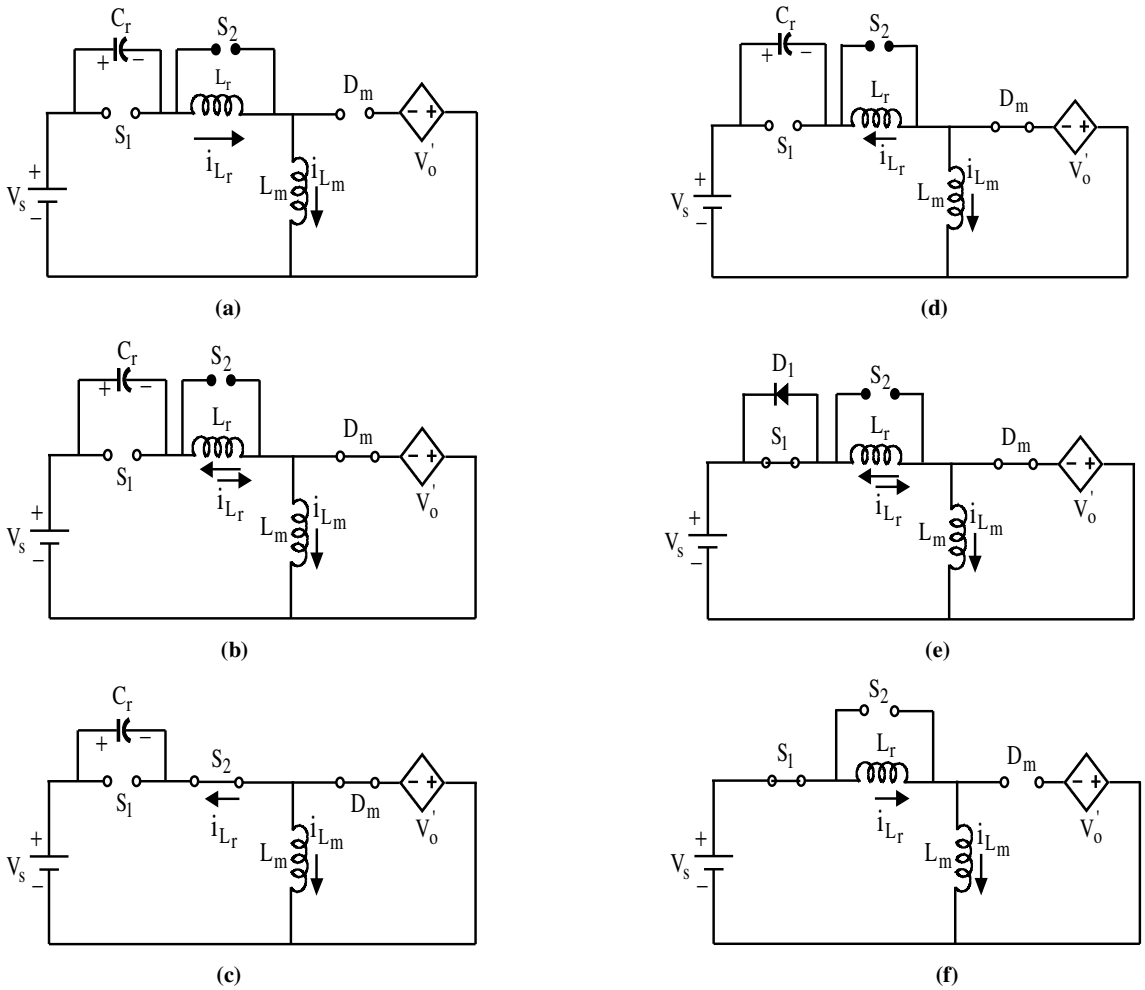

Fig.4(a-d). Equivalent circuit of flyback ZVS-QRC in six topological stages (a-d) of a switching cycle.

$$i_{L_r}(t) = -I_M \cos \omega_o t \quad (19)$$

$$v_{C_r}(t) = (V_s + V_o') - I_M Z_o \sin \omega_o t \quad (20)$$

This stage terminates when $v_{C_r}(t)$ becomes zero. Beyond t_4, the diode D_1 clamps v_{C_r} to zero. The duration of this stage is T_{d4} which is equal to t_4-t_3 and it is given by

$$T_{d4} = \left(\frac{1}{\omega_o}\right) \arcsin\left[\frac{(V_s+V_o')}{I_M Z_o}\right] \quad (21)$$

$$T_{d4} = (\alpha - \pi)/\omega_o \quad (22)$$

where $\alpha = \pi + \arcsin\left(\frac{V_s+V_o'}{I_M Z_o}\right)$ (23)

and α lies in the range of $\pi < \alpha < 3\pi/2$. The inductor current $i_{L_r}(t)$ at $t = t_4$ is given by

$$i_{L_r}(t_4) = -I_M \cos\alpha \quad (24)$$

2.5. Linear Inductor Charging Stage ($t_4 \leq t < t_5$)

The switch S_1 is turned ON when $v_{C_r}(t)$ becomes zero at $t = t_4$, to achieve zero voltage switching (ZVS). During this stage, the current i_{L_r} increases linearly and reaches the value I_M at $t = t_5$.The circuit diagram of this stage is shown in fig.4(e). Beyond t_4, the capacitor voltage is clamped to zero by the diode D_1. The corresponding state equation is

$$L_r \frac{di_{L_r}}{dt} = (V_s + V_o') \quad (25)$$

with initial condition, $i_{L_r}(t_4) = -I_M \cos\alpha$, the resonant inductor current is derived and it is given by

$$i_{L_r} = \left[\frac{(V_s+V_o')t}{L_r}\right] - I_M \cos\alpha \quad (26)$$

This stage terminates, when inductor current $i_{L_r}(t)$ becomes I_M. The duration of this stage is given by

$$T_{d5} = t_5 - t_4 \quad (27)$$

$$T_{d5} = \frac{I_M Z_o}{(V_s+V_0')\omega_o}(1+\cos\alpha) \quad (28)$$

2.6. Constant Current Stage ($t_5 \leq t < t_6$)

Once the resonant inductor current $i_{L_r}(t)$ reaches I_M at $t = t_5$, the freewheeling diode D_m turns OFF as shown in fig.4(f) . The switch S_1 carries current I_M as long as it is kept on until t_6.By varying the duration of this stage, the output voltage V_o' can be controlled. At t_6, the switch S_1 is turned OFF which starts the new cycle. The duration of this stage is T_{d6} which is equal to t_6-t_5.

$$T_{d6} = T_s - (T_{d1} + T_{d2} + T_{d3} + T_{d4} + T_{d5}) \quad (29)$$

The voltage conversion ratio, M_k of multi-output flyback ZVS-QRC when referred to secondary side is given by

$$M_k = \frac{V_{ok}}{V_s} = \left[1 - \frac{1}{\frac{f_s}{2\pi f_o}\left[\alpha + \frac{R_k}{2n_k M_k} + \frac{M_k n_k}{R_k}(1-\cos\alpha)\right] + \frac{T_{d3}}{T_s}}\right] n_k \quad (30)$$

where $R_k = R_{ok}/Z_o$ and k=1,2. In this work, it is proposed to maintain the voltage transfer gain M_1 constant against load or input voltage changes by controlling the switching frequency and setting

T_{d3} at 1.2µsec. This in turn reduces control range of frequencies required to regulate output voltage V_{o1} when compared to FM-ZVS-QRC.

From fig.6 and fig.7 it is observed that the conversion ratios M_1 and M_2 are sensitive to load changes. Hence, a closed-loop control system is necessary. In this work, it is proposed to achieve a voltage regulation of sensitive output (V_{o1}) by the proposed FM and inductor freewheeling technique control using TMS320F2407A DSP and the other output voltage, V_{o2} is cross-regulated. It is observed from fig.6, for change in conversion ratio(M_1) of ± 0.05, there is change in switching frequency within ±7 KHz.The design procedure of multi-output flyback ZVS-QRC operating in continuous conduction mode (CCM) is given with following specifications:

Maximum input voltage	$V_{s,\,max}$	= 14V
Minimum input voltage	$V_{s,\,min}$	= 10V
Output voltages	V_{o1}	= 5V
	V_{o2}	= 12V
Rated load current 1	I_{o1}	= 1A
Rated load current 2	I_{o2}	= 0.5A
Switching frequency	f_s	= 100 kHz

Transformer Ratings:

Volt-Ampere rating=	25 VA	
V_p (RMS)	=	8.66 V
V_{S1} (RMS)	=	3.535 V
Turns ratio n_1	=	0.42
n_2	=	1

(i)(a) The range of voltage conversion ratio for secondary1, M_1

$$M_{1,min} = \frac{V_{o1}}{V_{s,max}} = 0.3571$$

$$M_{1,max} = \frac{V_{o2}}{V_{s,min}} = 0.5$$

(b) The range of voltage conversion ratio for secondary2, M_2

$$M_{2,min} = \frac{V_{o2}}{V_{s,max}} = 0.857$$

$$M_{2,max} = \frac{V_{o2}}{V_{s,max}} = 1.2$$

(ii)The switching frequency (f_s) and resonant components

Selecting normalised frequency, f_{ns} as 0.15, the resonant frequency is selected as $f_o = f_s/(0.15) = 667$ kHz. The resonant components L_r and C_r are calculated using equations (1), (3) and (31) by ignoring the leakage inductances in the transformer. The condition for zero voltage switching is given by

$$I_M Z_o > (V_s + V_o') \qquad (31)$$

Hence, maximum magnetizing current I_M at nominal load

$$I_M = (M_{max} + 1)I_o = 1.84A$$

where $I_o = I_{o1}n_1 + I_{o2}n_2$ and $M_{max} = \frac{V_o'}{V_s}$. Therefore to satisfy equation (31), $Z_o > 13\Omega$. Using Z_o and f_o values, L_r and C_r are calculated as 7.636µH and 0.007µF respectively.

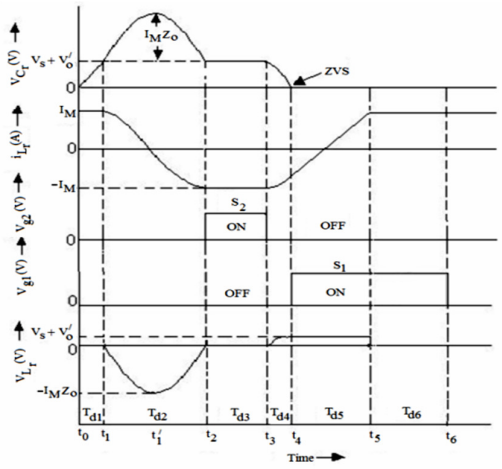

Fig.5. Theoretical resonant waveforms of multi-output flyback ZVS-QRC.

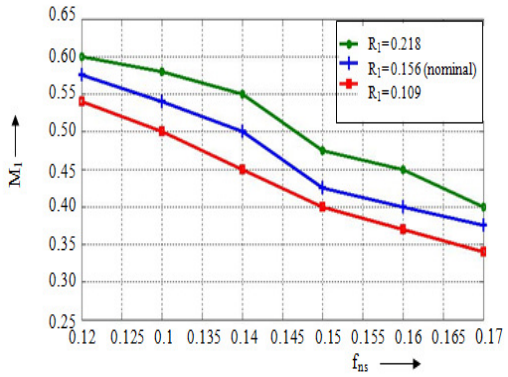

Fig.6. Control characteristics of M_1 versus f_{ns} for multi-output flyback ZVS-QRC for T_{d3}=1.2µsec.

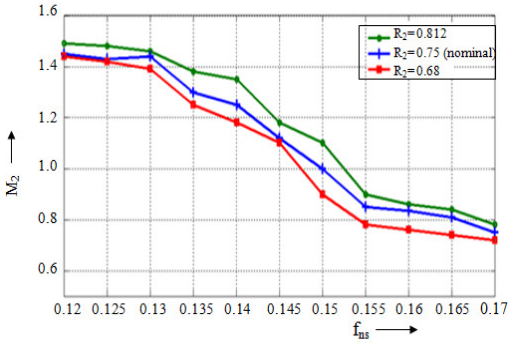

Fig.7. Control characteristics of M_2 versus f_{ns} for multi-output flyback ZVS-QRC for T_{d3}=1.2µsec.

3. IMPLEMENTATION OF PROTOTYPE MULTI-OUTPUT FLYBACK ZVS-QRC

An experimental set-up of multi-output flyback ZVS-QRC as shown in fig.8 is implemented with following parameters: V_s = 12V, V_{o1} = 5V, V_{o2} = 12V, f_s = 100kHz, L_r = 7.636µH C_r = 0.007µF, R_{o1}=5Ω, R_{o2} = 24Ω. The resonant inductor is made of ferrite core and the capacitors are of plain polyester. Power MOSFETs IRF540 are used as active switches S_1 and S_2 and fast recovery diode FR107 is used as freewheeling diode D_m. The snapshot of the closed-loop

experimental set-up is shown in fig.9. The gating pulses to switches S_1 and S_2 are generated using event manager module, available in TMS320F2407A 16 bit, 40 MHz DSP.

The PWM signal from the DSP is not capable of directly driving the MOSFET. In order to strengthen the triggering pulses and to provide isolation between the control circuit and power circuit, a separate opto-coupler MCT2e and driver circuit is provided as shown in fig.8. The 10-bit ADC unit present in processor accepts maximum analog input voltage of 3.5V.The conversion time of ADC is 375nsec. It converts maximum of 16 multiplexed analog inputs. The load currents (I_{o1} and I_{o2}) are sensed by LP25-NP which is a closed-loop (compensated) multi-range current transducer using the Hall effect. During closed-loop operation the converter output voltages (V_{o1} and V_{o2}) and load currents (I_{o1} and I_{o2}) are scaled down to 3.5V using HCPL7840 analog amplifier.

The output waveforms are captured by waveform analyser software which is a proprietary and comprehensive software environment used to acquire the serial digital data via Communication port and input the data through USB port to PC. The data acquired via USB port will be plotted in windows form with appropriate scales in X and Y axes in single scope as well as dual scope modes.

In closed-loop operation, variable frequency control modulates the ON time of switch S_1 and OFF time of switch S_2. If the output voltage is reduced due to increased load current, the normalised switching frequency (f_{ns}) is decreased in order to increase the effective ON period and OFF period of switch S_1 and S_2, respectively.

3.1 Open Loop Experimental Results

The experimental resonant waveforms are shown in fig.10 and fig.11. It is observed that the switch S_1 is turned ON, when the resonant capacitor voltage becomes zero to assure ZVS condition.

The unregulated output voltages V_{o1} and V_{o2} along with their load currents I_{o1} and I_{o2} of secondary 1 and 2 for 20% step decrease in load resistance (R_{o1}) are shown in fig.12 and fig.13. It is observed that the output voltage V_{o1} deviates from its nominal value of 5V and settles at 4.5V. Also the other output voltage V_{o2} deviates from its nominal value of 12V and settles at 10V. It is observed that a closed-loop system is needed to regulate the output voltage of secondary 1 (V_{o1}) against load disturbances by FM technique and the output voltage of secondary 2 (V_{o2}) is cross regulated.

3.2 Experimental Results for Closed-Loop Control with PI

Fig.14 shows the regulated output voltage (V_{o1}) of secondary 1 and cross-regulated output voltage (V_{o2}) of secondary 2 for 20% step decrease in load resistance (R_{o1}) with PI controller. A change in the output voltage level due to load variations triggers the PI controller to reach the nominal output voltage of the converter by modifying the duty cycle of the PWM signals, which is applied to MOSFET switches S_1 and S_2 of multi-output flyback ZVS-QRC. The conventional PI controller parameters are obtained by Z-N open loop method as proportional gain K_c=3.4 and integral gain K_i = 1.0. From the experimental waveform shown in fig.14, it is observed that the output voltage of secondary 1 (V_{o1}) is well regulated and settles at its reference voltage 5V within 17msec and output voltage of secondary 2 (V_{o2}) is also cross-regulated within 20msec for step decrease in load resistance (R_{o1}) of 20%.

However, PI controllers are sensitive to operating point and parameter variations. The complex structure and non-linear characteristics of QRC necessitates the design of non-linear control. Hence in this work, an attempt is made to design a fuzzy logic controller for the proposed converter to regulate the output voltage against load variations.

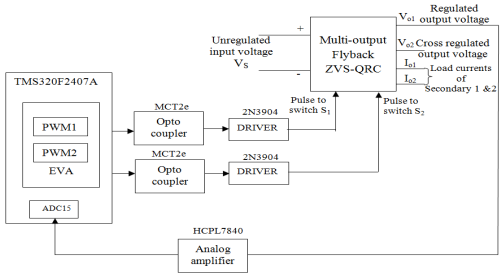

Fig.8. Closed-loop experimental set-up for multi-output flyback ZVS-QRC.

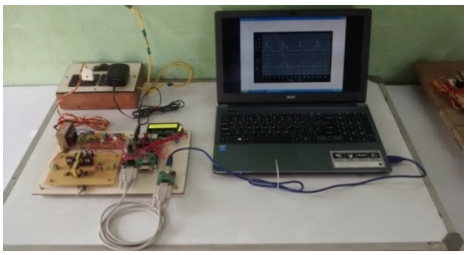

Fig.9. Photocopy of prototype model of multi-output flyback ZVS-QRC.

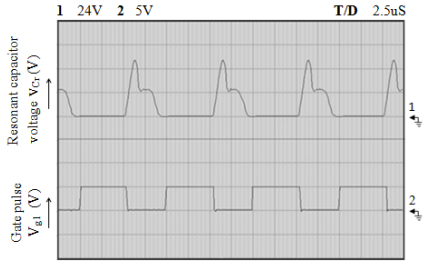

Fig.10. Resonant capacitor voltage(V_{Cr}) and main switch pulse (V_{g1}).

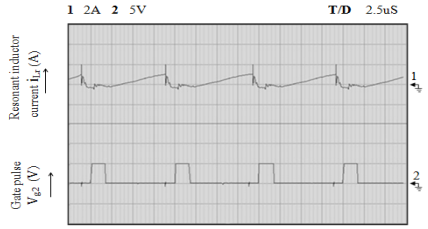

Fig.11. Resonant inductor current (i_{Lr}) and auxiliary switch pulse (V_{g2}).

3.3 Experimental Results for Closed-Loop Control with CFLC

The inputs to the CFLC are the error voltage(e) and change in error(ce). The output is the change in switching frequency(Δu). Depending on the magnitude and sign of e and ce, the switching frequency of the main switch S_1 and auxiliary switch S_2 is varied to regulate the output voltage. For ease of computation, the variables are divided into five fuzzy subsets using triangular membership function as shown in fig.15. **T**he CFLC acts effectively and forces the converter output voltage of secondary 1, V_{o1} to follow the reference voltage of 5V with settling time of 12msec and the output voltage of secondary 2, V_{o2} is cross regulated well within nearly 12 msec as shown in fig.16 for 20% step decrease in load resistance (R_{o1})

4. CONCLUSIONS

The detailed analyses of various stages of operation and the design procedure of multi-output flyback ZVS-QRC have been presented. The performance measures of closed-loop control of multi-output flyback ZVS-QRC for various controllers like PI and CFLC from experimental studies have been compared and tabulated in Table 2. From the table 2 it is observed that CFLC performs better than PI controller in terms of low offset, less settling time, low ISE value.

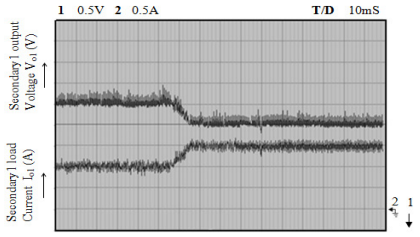

Fig.12. Unregulated experimental output voltage (V_{o1}) and current (I_{o1}) of secondary 1 for 20% step decrease in load resistance (R_{o1}).

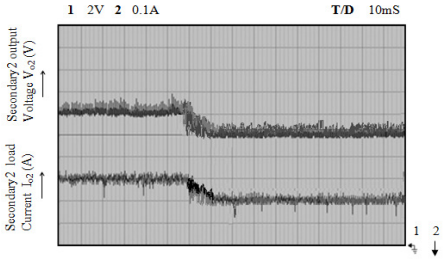

Fig.13. Unregulated experimental output voltage (V_{o2}) and current (I_{o2}) of secondary 2 for 20% step decrease in load current (R_{o1}).

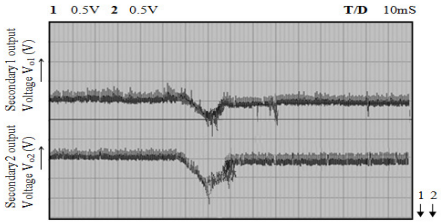

Fig.14. Regulated experimental output voltage (V_{o1}) of secondary 1 and cross-regulated output voltage (V_{o2}) of secondary 2 for 20% step decrease in load resistance (R_{o1}) with PI controller.

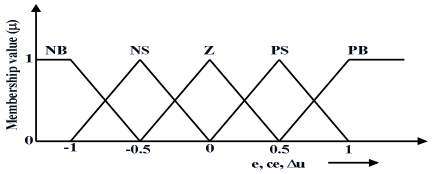

Fig.15. Membership function diagram of e, ce and Δu.

Table 1. CFLC control rules for multi-output flyback ZVS- QRC.

e \ ce	NB	NS	Z	PS	PB
NB	NB	NB	NS	NS	Z
NS	NB	NS	NS	Z	PS
Z	NS	NS	Z	PS	PS
PS	NS	Z	PS	PS	PB
PB	Z	PS	PS	PB	PB

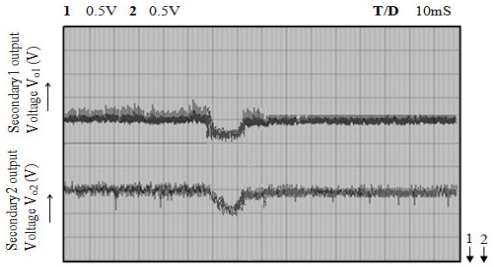

Fig.16. Regulated experimental output voltage (V_{o1}) of secondary 1and cross-regulated output voltage (V_{o2}) of secondary 2 for 20% step decrease in load resistance (R_{o1}) with CFLC.

Table 3. Performance measures of multi-output flyback ZVS-QRC from experimental studies.

	PI controller		**Fuzzy logic controller (CFLC)**	
Load variations	20% step decrease in R_{o1}	20% step increase in R_{o1}	20% step decrease in R_{o1}	20% step increase in R_{o1}
Offset	0.04	0.04	0.01	0.01
Settling time (msec)	17	17	12	12

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