5-READ 2-WRITE MULTIPORT REGISTER FILE DESIGN USING NOVEL D-LATCHES

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Abstract:

Memory devices are crucial components in the design of various applications, and historically, SRAMs have been widely used. However, SRAMs come with limitations, primarily allowing only 1-READ and 1-WRITE operations. To overcome this limitation, multi-port registers have become popular, offering the ability to carry out multiple read and write operations simultaneously. Pulsed latches are often employed in multi-port registers due to their excellent performance and minimal power consumption. Compared to SRAM-based register files, register files utilizing pulsed latches have shown significant reductions in both space and power consumption. In the context of 180nm technology, a novel approach involves designing an 8-bit multi-port register file based on d-latches, capable of 5-READ and 2-WRITE operations. This design was simulated and its power consumption examined using tools like Microwind. Such advancements in register file design contribute to improved efficiency and performance in various electronic systems.

Introduction:

The register file is a crucial component in modern processors, providing fast access to data for the execution units. As processors become more complex and demanding in terms of performance, the design of the register file becomes increasingly challenging. One key challenge is to provide multiple read and write ports to support the parallelism required by modern applications while maintaining low power consumption.

In this paper, a novel design was proposed using 5 transistors. This D-latch utilizes a modified latch structure that reduces power consumption compared to traditional designs. NOR based pulser has been designed to generate 7 pulses consisting of 5 read and 2 write pulses. Multiport Register file is implemented using designed Novel D Latch & NOR based pulser which can perform 5 read and 2 write operations.

Related Works:

J. Kadomoto [1] This paper addresses the demand for higher performance in embedded SoCs by exploring multiport register file design for 32-bit out-of-order superscalar processors. It emphasizes the need for efficient utilization of internal memory structures amidst increasing parallel execution lanes. Through SPICE simulations, the study delves into the intricate design space, crucial for developing higher-performance cores while managing power consumption and complexity.

Manivannan [2] presented a study focusing on the efficiency of pulsed-latches combined with flip-flops for improved performance and reduced power consumption, particularly for multi-read and multi-write operations. Their design targets area efficiency and lower power consumption compared to conventional SRAM-based register files. They highlight the quadratic increase in space for SRAM-based multiport register files with capacities larger than 128KB due to the implementation of four READ ports per cell.

Adam Teman [3] proposed a novel approach utilizing industry-standard transistor models for quick separatrix tracing in various SRAM configurations. With increasing memory density, accurate examination of SRAM stability becomes crucial, as conventional measurements may fail to capture dynamic SRAM behavior, leading to costly design errors.

Wael M. Elsharkasy [4] briefly examined different register file implementations, noting a preference for pulsed latch solutions for small-sized register files. They compared conventional 1R1W register file implementations utilizing SRAM and flip-flops and introduced a novel pulsed latch implementation with virtual ports, which exhibited significant power and area reductions compared to previous methods.

Khawar Sarfraz [5] suggested a 4-transistor read port architecture aiming for a low-read-power design capable of operating at frequencies exceeding 3 GHz. Their design incorporates precharge buffer and dynamic local bitline components, with improved resilience demonstrated by the low Vt local bitline. Measurement results on a 65-nm test chip showed promising read-out speed and reduced power consumption.

Shen-Fu Hsiao [6] presented methods for designing low-cost, low-leakage multi-port SRAM for register files in a vertex shader processor. They utilized power-gating, dynamic forward body-bias control, and recharge control to minimize leakage and unnecessary processes. Their layout design features thin-cell-like structures and asymmetric cross-coupled inverters to optimize area and writability, showing improvements over existing designs in terms of space and leakage.

Shenglong Li [7] introduced a full custom design for a multi-port register file supporting multiple write and read operations. Their design enables read-after-write access within a single system cycle, incorporating synchronous read and asynchronous write mechanisms. Implemented in SMIC 0.13μm CMOS technology, the register file demonstrated satisfactory performance and power consumption under worst-case conditions.

Shermina M. Meera [8] presented a 5-transistor SET D flip-flop implemented across various scaling technologies from 180 nm to 50 nm. It presents a comparison of area and power dissipation among several technologies, emphasising notable improvements in both areas. The effectiveness of the entirely custom approach is demonstrated by simulation results, which show a 39% reduction in area and a 37% reduction in power when compared to fully automatic design.

S. Trotta [9] introduced an innovative asymmetric D-latch design, emphasizing its performance at high frequencies The behaviour of the circuit, especially its potential for speed enhancement, is shown through analysis and simulations. The flip-flops stand out for having dynamic efficiency at high frequencies and static stability at low frequencies. In the end, the design's benefits, drawbacks, and performance are assessed using real-world IC measurements, particularly in the context of a pseudo random bit sequencer application.

PROPOSED DESIGN METHODOLOGY:

This section presents a NOR-based pulser that replaces a two-input NAND gate, with a delay unit linked to one input. Seven non overlapping pulse signals are necessary per clock cycle. For this seven pulse generators are employed with each subsequent one receiving the delayed clock input from the preceding unit. Five unique pulse signals (A, B, C, D, and E) are required for a 5-read operation. These pulse signals are then combined with the address bits for each read operation through AND gates.

NOR Based Pulser:

To reduce power consumption, the two-input NAND gate, with a delay unit attached to one of its inputs, has been replaced with a NOR gate as depicted in Fig. 10. The clock signal is provided as input to the NOR gate, causing the difference between the clock and the delayed clock to form a pulse signal at the NOR gate's output. The NOR gate generates the pulse relative to the negative edge of the clock.

Novel D Latch:

In the novel D latch design, comprising five transistors, including one each for D, CLK, and Q, M1 and M4 initially deactivate. Subsequently, during CLK's low state, M2, M3, and M5 activate. Conversely, when D is high, M2, M3, and M4 are inactive, while M5 remains operational. Upon a high-to-low transition in CLK, M1 and M4 activate. The output Q is generated from this configuration.

TABLE 1: Truth Table of Novel D Latch

CLK	D	OUT
0	X	OUT(HOLD)
1	0	0(RESET)
1	1	1(SET)

8 Bit Multiport Register File:

An 8-bit multiport register using 5T D-latches is a fundamental component in digital circuit design, offering efficient data storage and retrieval capabilities. Each 5T D-latch is a basic memory element comprising five transistors, typically implemented using CMOS technology. In an 8-bit register, eight such latches are interconnected to form a storage unit capable of holding 8 bits of data.

The register can be used for various purposes, including temporary storage of data during computation, buffering of input or output data, or as part of a larger memory hierarchy. The 5T D-latches in the register allow for both parallel loading of all 8 bits and serial input and output operations, providing flexibility in data manipulation.

However, once properly designed and implemented, such a register can provide reliable and

efficient data storage functionality in a wide range of digital systems.

Simulation results:

The entire existing and proposed design was implemented using microwind tool in 180nm technology. Analysis was performed to verify READ and WRITE operations. Power consumption is also calculated for various supply voltages (VDD). Table 2, Table 3 shows the Comparison of Power for Existing & Proposed Multiport Register File. Fig. 1 & Fig. 2 represent the bar graph for respective tables..

TABLE 2: Comparison of Power for Existing & Proposed Multiport Register File

VDD(v)	Power(µW) 4-READ & 2-WRITE (Existing circuit)	Power(µW) 4-READ & 2-WRITE (Proposed circuit)
0.70	115.36	105.9
0.80	169.5	163.58
0.90	252.9	213.14
1.00	515.7	285.21
1.10	754.6	416.64
1.20	989.7	441.87

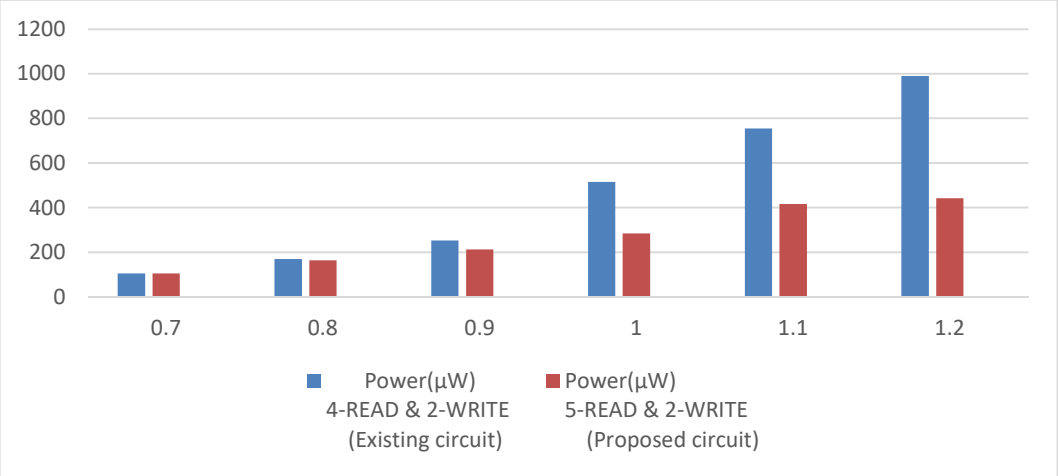

Fig.1: Represents Comparison of Power for Existing & Proposed Multiport Register File

TABLE 3: Comparison of Power for Existing & Proposed 5 READ Multiport Register File

VDD(V)	Power(µW) 4-READ & 2-WRITE (Existing circuit)	Power(µW) 5-READ & 2-WRITE (Proposed circuit)
0.70	105.9	78.80
0.80	169.5	171.26
0.90	252.9	237.28
1.00	515.7	301.632
1.10	754.6	418.72
1.20	989.7	509.42

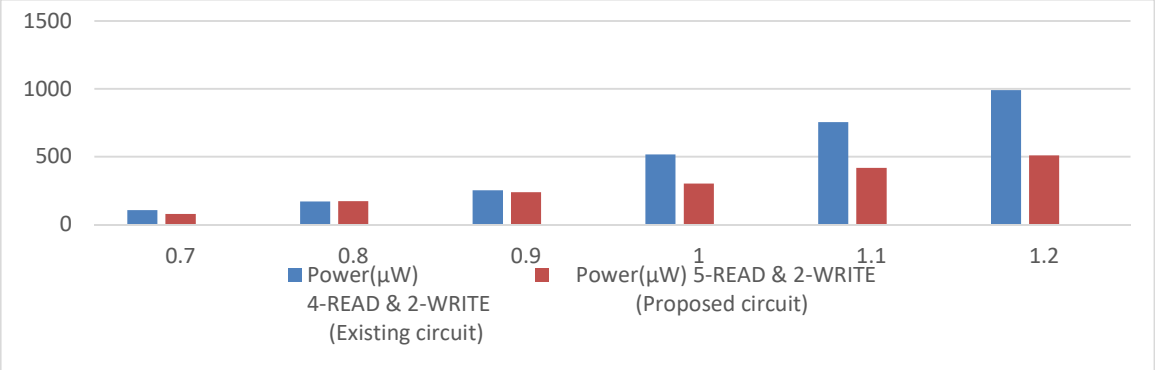

Fig.2: Represents Comparison of Power for Existing & Proposed 5 READ Multiport Register File

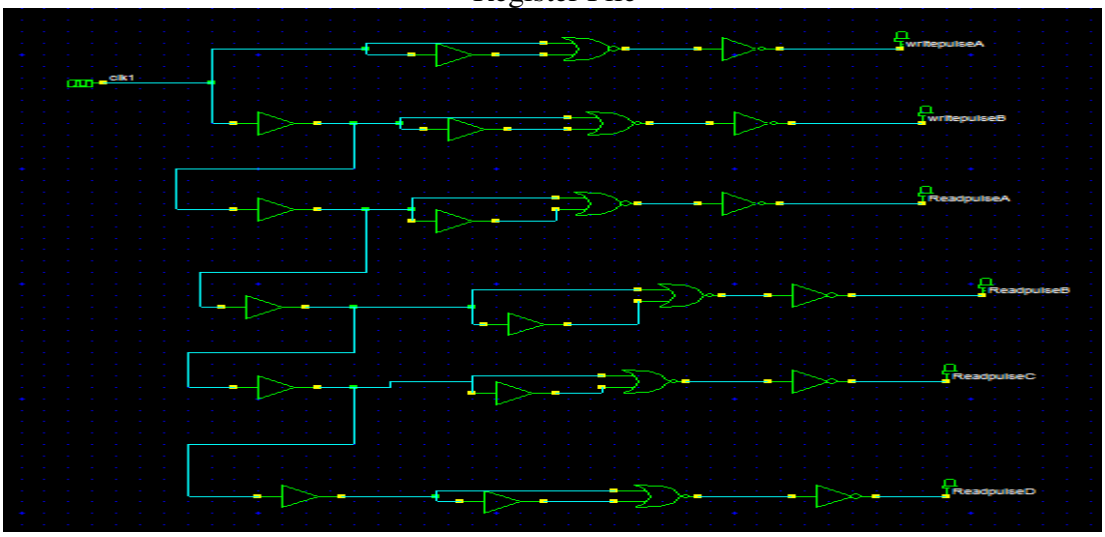

Fig.3: Schematic diagram of NOR Based Pulser in DSCH 3.9

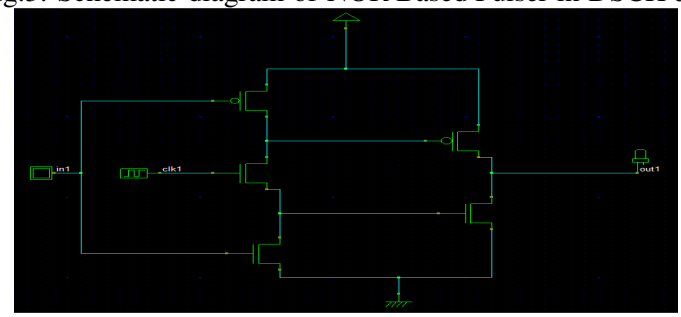

Fig.4: Schematic diagram of Novel D Latch in DSCH 3.9

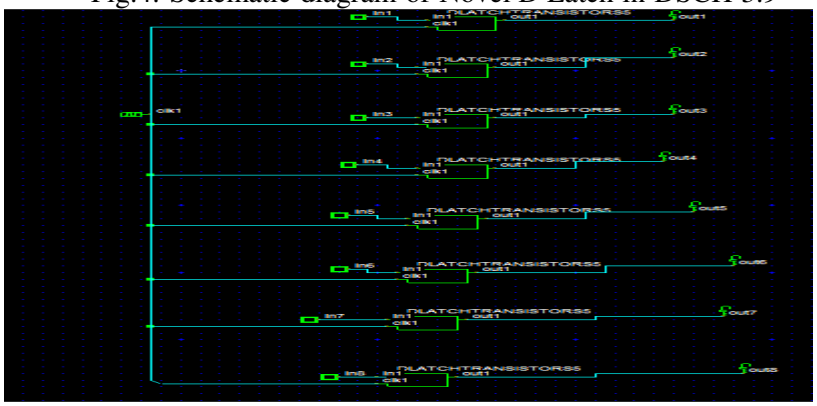

Fig.5: Schematic diagram of 8 Bit Multiport Register File in DSCH 3.9

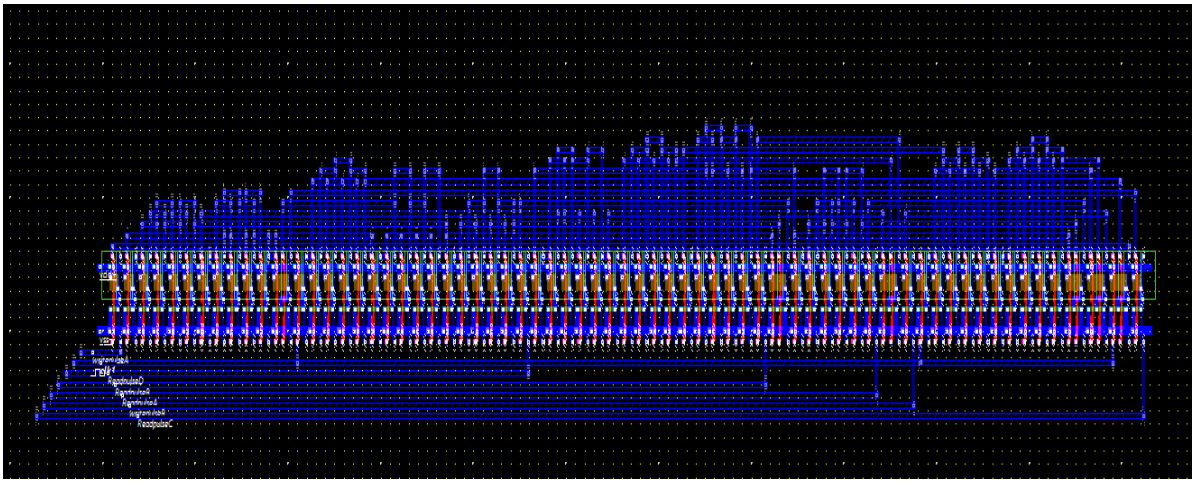

Fig. 6: Layout of NOR Based Pulser

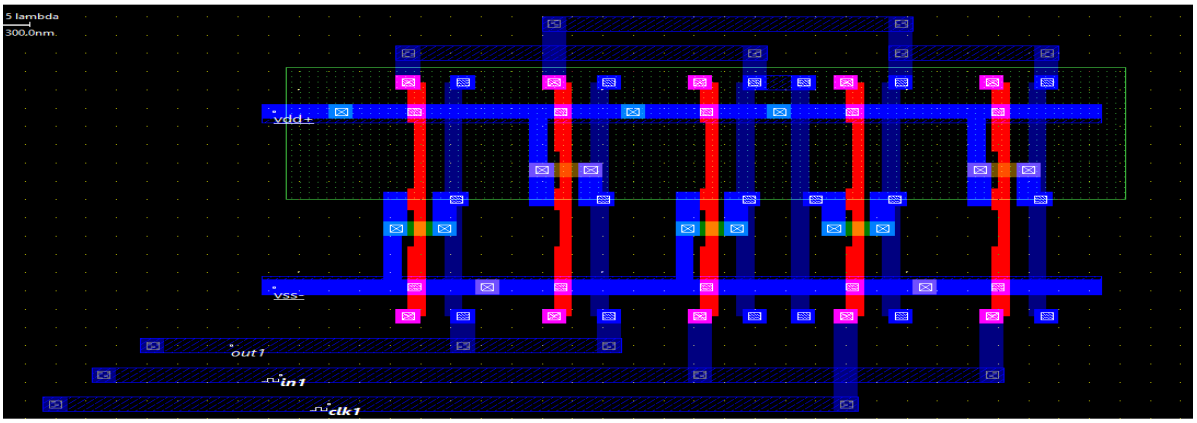

Fig. 7: Layout of Novel D Latch

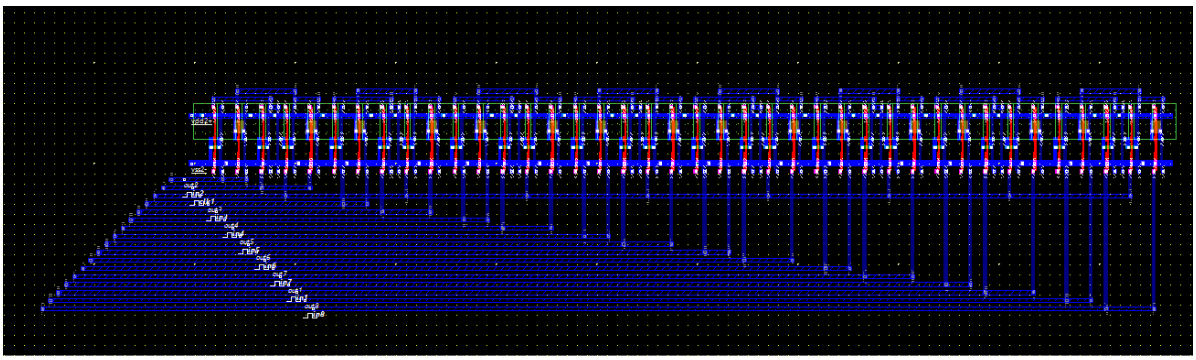

Fig. 8: Layout of 8 Bit Multiport Register File

CONCLUSION:

In summary, the re designed 8-bit register achieves significant power reduction through strategic optimizations. Increased READ logic units contribute 50% decrease in power consumption. Transitioning from NAND to NOR pulsers yields an additional 10% reduction in power. Notably, latch units shows 60% decrease in power consumption, with an improved D latch design. Despite a slight 6% decrease in READ logic power, overall savings are substantial. Variations in delay units further optimize power usage. These overall measures collectively result 50% reduction in power consumption, demonstrating a commitment to efficiency and sustainability while enhancing performance.

REFERENCES:

1. J. Kadomoto, H. Irie and S. Sakai, "Multiport Register File Design for High-Performance Embedded Cores," 2021 IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Singapore, Singapore, 2021, pp. 281-286, doi: 10.1109/MCSoC51149.2021.00048.

2. Adam Teman, Member, IEEE, and Roman Visotsky, A Fast Modular Method for True Variation-Aware Separatrix Tracing in Nano scaled SRAMs, IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS, 10, OCTOBER 2015.

3. Wael M. Elsharkasy, Hasan Erdem Yantir and Amin Khajeh, Efficient Pulsed-Latch Implementation for Multiport Register Files, 2017 ACM.

4. Khawar Sarfraz and Mansun Chan, A 1.2V-to-0.4V 3.2GHz-to-14.3MHz Power-Efficient 3-Port Register File in 65-nm CMOS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, April 23, 2016.

5. Shen-Fu Hsiao and Pu-Cheng Wu, Design of Low-Leakage Multi-Port SRAM for Register File in Graphics Processing Unit, 2014 IEEE.

6. Shenglong Li, Zhaolin Li and Fang Wang, Design of A High-Speed Low-Power Multiport Register File, 2009 IEEE.

7. Meera Shermina .M, Meera Shahanaz. M, Nampoothiri Nishi G., International Journal of Advance Research, Ideas and Innovations in Technology.

8. S. Trotta, J. Sundermeyer, N. Weber and J. Saurer, "A novel design of an asymmetric D-latch," Digest of Papers. 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems,2004., Atlanta, GA, USA, 2004, pp. 261-264, DOI: 10.1109/SMIC.2004.1398218.

9. B. Chinnarai, B Fransis, Y. Apparao, “Design of A Low Power Flip-Flop Using CMOS Deep Submicron Technology,” International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, Vol-2 Iss-1, pp. 95-99, 2012.

10. Z Chen, M Johnson, L Wei, and K Roy, “A Novel Design of SET Flip Flop,” Tata McGraw-Hill publication New Delhi, pp. 343-344, 2010 [3] T. Thangam, P. Jeya Priyanka, V. Sangeetha, “Performance Improved Low Power D-Flip Flop with Pass Transistor Design and its Comparative Study” IJISET- Vol. 2 Issue 4, April 2015.

11. Noble G, Sakthivel S.M, “A Novel Flip-Flop Design for Low Power Clocking System,” International conference on Communication and Signal Processing, April 3-5, 2013, India, ©2013 IEEE [12]. N. Nishanth, B. Sathyabhama, “Design of Low Power Sequential Circuit Using Clocked Pair Shared Flip flop,” 2013 IEEE International Conference on Emerging Trends in Computing,

Communication, and Nanotechnology (ICECCN 2013).

13. Ulrich Tietze, Christoph Schenk, Halbleiter-Schaltungstechnik.12, Auflage, “Transmission gate” Springer, Berlin/Heidelberg/New York 2002, ISBN 3-540-42849-6.

14. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits,” Tata McGraw-Hill publication New Delhi, pp. 343-347, 2010.

15. Praveen Kumar Chakravarti, Rajesh Mehra, “Layout design of D Flip Flop for Power and Area Reduction,” International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882 EATHD-2015 Conference Proceeding, 14-15 March 2015.

16. J. Scott, 1. H. Lee, J. Arends, B. Moyer, "Designing the low-power micro-architecture," IEEE Power Driven Micro-architecture Workshop, 1998.
17. V. Zyuban, P. Kogge, "The energy complexity of register files," ISLPED, pp.305-310, Aug.1998. [3] C. Asato, "A 14-port 3.8ns 116-word 64b read-renaming register file," IEEE J of Sold-State Circuits, pp. 1254-1258, Nov.1995.

18. N. T. zartzanis, W. W. Walker, "A differential current-mode sensing method for high-noise-immunity, single-ended register files," Digest of Technical Papers, ISSCC IEEE International Solid-State Circuits Conference, pp. 1505-1521,2004.

19. Q. Yu, D. Wang, T. Zhang, "A design of 500MHz lO-read 6-write register file;' The 6th International Conference on ASIC, ASICON, pp. 311-316, Oct. 2005.

20. H. Nambu, et al., "A 1.8 ns access, 550 MHz 4.5 Mb CMOS SRAM;' IEEE Journal of Solid-State Circuits, pp. 1650-1658,1998.33(11).

21. M. M. Khellah and M. I. Elmasry, "Circuit Techniques for High-Speed and Low-Power Multi-Port SRAMs; ' Eleventh Annual IEEE International ASIC Conference, 1998, Rochester, NY, USA.