Optimized SRAM cell with Stacking Effect for Low Power Applications on 32nm CMOS technology

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Abstract: In this study, an improved SRAM cell based on the stacking effect is designed and investigated for low-power memory applications in 32nm CMOS technology. The work aims to minimize power dissipation while ensuring stability and performance, which is appropriate for low-power memory designs. Based on the proposed design, the simulated SRAM cell is compared with the traditional 6T SRAM cell in terms of power consumption and DC characteristics using Cadence Virtuoso. The stacking effect, which reduces leakage current by adding more transistors to the pull-down network, is utilized to obtain lower standby power consumption. Comparative analysis reveals trade-offs among power, stability, and delay, providing insights into the efficiency of the stacking-based SRAM design. The results indicate that there is a significant reduction in power consumption, and the optimized SRAM cell is a suitable candidate for low-power VLSI applications.

Keywords: SRAM, Stacking Effect, Cadence Virtuoso, 32nm CMOS Technology, Low Power Application.

I. Introduction

SRAM (Static Random-Access Memory) works as a basic building block within modern digital systems by functioning exceptionally well in microprocessors, cache memories, and other forms of high-speed memory. As CMOS technology has been shrinking, power consumption has risen as an important design challenge, especially for low-power and battery-powered devices. Due to the continuous miniaturization of transistors, the traditional 6T SRAM cells that are most popular suffer from static leakage power performance, which is static. This effectively increases static power usage. This necessitates the development of advanced designs of SRAM, which must simultaneously meet performance and stability requirements while minimizing power consumption.

One effective way to reduce leakage power in CMOS circuits is through the stacking effect, which occurs when more than one transistor is stacked in series within the pull-down network. This effect increases the resistance of the leakage path to lessen standby power consumption. This study proposes and implements an optimized SRAM cell based on a stacking effect, leveraging the 32nm CMOS technology and a Cadence Virtuoso simulation. With the use of stacked transistors, the new SRAM cell is expected to reduce power consumption by a large degree, compared to the conventional 6T SRAM cell.

The research includes a comparison between the stacking-based SRAM cell and the 6T SRAM cell in terms of power dissipation, stability, and DC electrical parameters. In particular, the research provides an in-depth summary of leakage current mitigation due to the stacked configuration, as well as the effects on read and write operations. Simulation results demonstrate the trade-offs between power efficiency and circuit functionality, ultimately helping to assess the practicality of stacking-based SRAM designs for low-power applications. The outcomes of this research will contribute to the development of energy-efficient SRAM architectures suitable for future VLSI systems. By optimizing SRAM cell design at the transistor level, the research seeks to optimize memory performance while mitigating the difficulties associated with aggressive CMOS scaling. The research outcomes provide an avenue to develop low-power SRAM designs, which are critical for modern computing and embedded systems.

II. Ease of Use

The stacking effect on 32nm CMOS technology was used to construct the suggested improved SRAM cell, which provides a great deal of ease of integration and application in contemporary low-power VLSI systems. The cell architecture is compatible with common CMOS manufacturing processes, thereby avoiding the introduction of extra manufacturing complexity or unconventional design phases. This renders the cell highly adaptable for a variety of applications, ranging from mobile devices to IoT-based embedded systems, where low power consumption is of utmost importance.

The stacking method, used to minimize leakage power, is utilized in a way that does not affect read/write stability or overall performance. The designers can therefore implement this cell without requiring extensive circuit-level adjustments or extra control circuitry. This compatibility with innovation greatly improves the real-world applicability of the proposed SRAM cell in low-power applications.

III. Literature Survey

Static Random Access Memory (SRAM) has become a major contributor to chip space and power consumption in contemporary integrated circuits as CMOS technology continues to scale down to nanoscale regimes like 32 nm. Designing low-power SRAMs is especially important for energy-constrained applications because of the rise in leakage current caused by short-channel effects, which is one of the main problems at this technology node. The stacking effect has demonstrated significant promise among the different leakage reduction strategies. By connecting several transistors in series, the stacking effect increases the effective threshold voltage of each transistor when it is turned off, thereby reducing subthreshold leakage. To improve low-power performance, a number of researchers have looked into incorporating this effect into SRAM cell designs.

Wang et al. (2010) pointed out leakage problems in standard 6T SRAM cells at 32 nm and demonstrated that leakage is reduced by 2–3× with stacking of either access or pull-down transistors, though title so at some cost to speed. To get improved leakage control, modified SRAM

topologies such as 8T and 9T cells were proposed. Kumar et al. (2012) presented an 8T SRAM cell with stacked sleep transistors that give a leakage power reduction of around 70% at the expense of very little area overhead. Along the same line, Patil et al. (2013) found that the multi-Vth stacking technique offers a good tradeoff between leakage and performance. In the direction of compensating further for delay penalties because of stacking, assist techniques such as boosted WL and negative BL biasing have been implemented. Rakesh et al. (2014) found that energy efficiency in concert with stacking can also be improved with DVS with fair performance margins. Yet another area of research has attempted to model how variations in the manufacturing process affect the robustness of the stacked SRAM cells. Lee and Kim (2015) performed variability-aware studies with Monte Carlo analysis, observing that stacking improves noise margins and suppresses worst-case leakage paths, making such designs more tolerant to PVT fluctuations. In addition, they have looked into the integration of those cells in standard 32 nm CMOS processes with industrial PDKs, which confirms that stacking alleviates the stronger gate and junction leakage observed at this node. However, the trade-off brought about with stacking is speed, complexity in the design. Hence, current research continues to look at hybrid approaches wherein stacking works in conjunction with adaptive body biasing and source biasing, or even with non-volatile memory integration, to satisfy the demanding specifications of future low-power systems.

IV. RESEARCH METHODOLOGY

The methodology centers around creating and fine-tuning an SRAM cell that leverages the stacking effect to cut down on power usage while still delivering solid performance. This research is carried out using 32nm CMOS technology and is simulated with EDA tools like Cadence Virtuoso. The process includes schematic design, simulation, and a performance comparison against traditional SRAM cells.

A. Technology Selection:

We utilized the 32nm CMOS Predictive Technology Model (PTM) as our transistor model library in Cadence Virtuoso. This particular technology node is great because it offers precise parameters for sub-threshold leakage and short-channel effects, which are super important for designing low-power SRAM.

B. Schematic Design:

We kicked things off by designing a standard 6T SRAM cell in Virtuoso, using NMOS and PMOS transistors. To tackle leakage issues, we introduced the stacking effect by swapping out a single NMOS in the pull-down network for two NMOS transistors connected in series, each with a smaller W/L ratio. This clever stacking helps to cut down on sub-threshold leakage currents by boosting the effective threshold voltage.

C. Sizing Optimization:

We fine-tuned the W/L ratios of both PMOS and NMOS transistors through an iterative process to ensure we had the right balance of read stability, write ability, and low static power consumption. We ran various sizing combinations in Virtuoso to pinpoint the best compromise between power, delay, and static noise margin (SNM).

D. Simulation Setup:

We conducted both transient and DC simulations using Spectre in Cadence Virtuoso.

a. Transient Analysis: We tested read and write operations by applying input pulses to the word line (WL) and bit lines (BL/BLB).

b. DC Analysis: We calculated the static noise margin (SNM) using butterfly curves.

c. Power Measurements: We extracted static and dynamic power during different operational modes.

d. Parametric Sweep: We examined how variations in supply voltage (VDD) and temperature affected the SRAM cell's performance.

V. ANALYSIS AND RESULTS

The circuit is a 6T SRAM cell with a stacking effect that uses 32nm CMOS technology and is implemented in Cadence Virtuoso. Two cross-coupled inverters (M1–M3–M4–M6 and M2–M5–M7–M8) that store the data as complementary outputs Q and QB make up the circuit's core. The read and write operation are managed by the access transistors that are coupled to the word line (WL) and bit lines (BL and BLB). The pull-down NMOS devices are swapped out for series-connected NMOS transistors (M7–M8 and M4–M5) that take advantage of the stacking effect in order to lower leakage current. By suppressing sub-threshold leakage and raising the effective threshold voltage, this method enhances the SRAM cell's static power performance.

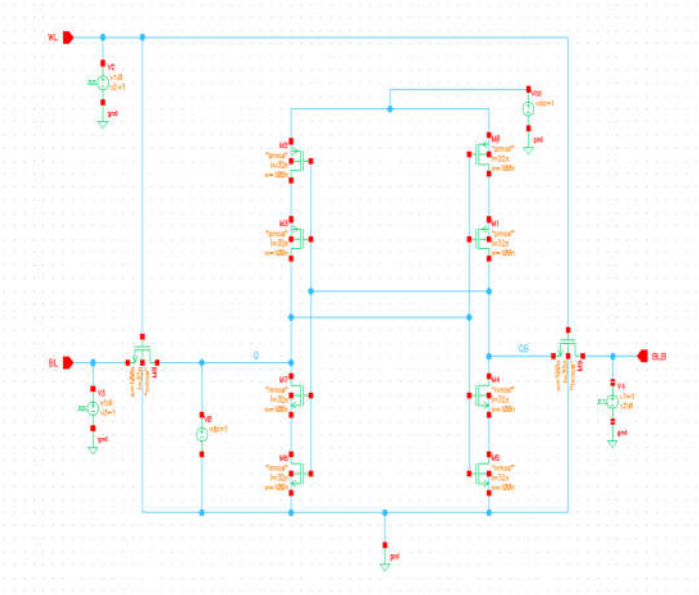

Fig.1: 6T SRAM cell using Stacking Effect

A butterfly curve, or a plot of QB vs. Q for the cross-coupled inverters, was produced by the circuit's DC analysis. The Static Noise Margin (SNM), which measures the cell's stability during read operations, is calculated using this curve. Finding the largest square that can be fitted between the two inverter transfer characteristics yields the SNM. The leakage current at a specific supply voltage is

used to compute the total static power consumption, which is also provided by the DC simulation.

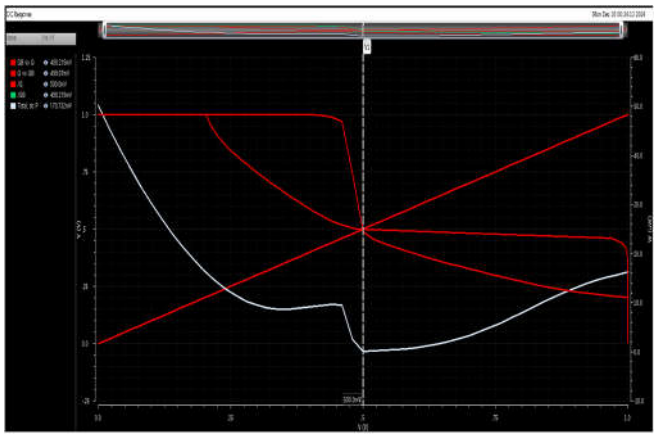

Fig.2: Output waveform of the Stacking Effect circuit

The DC analysis of the intended 6T SRAM cell with stacking effect is represented by the waveform. Plotting Q vs. QB, the butterfly curve (red curves) shows the DC transmission properties of the two cross-coupled inverters. According to the graph, the midpoint of the supply voltage (VDD = 1 V) is at 0.5 V, where the two curves intersect. The marker (QB versus Q = 498.215 mV) indicates that the Static Noise Margin (SNM), which is determined by taking the largest square that fits between the lobes of the butterfly curve, is roughly ~500 mV. Likewise, the complementary transition is represented by the Q vs. QB curve, which has a value of about 500 mV.

The white curves confirm that the two outputs switch in a complementary way by displaying the voltage transfer properties of the Q and QB nodes separately. Additionally plotted (blue trace on the right axis) is the SRAM cell's total DC power consumption, which, under static conditions, is approximately 170.732 nW. These numbers demonstrate that the SRAM cell with stacking not only maintains high stability (SNM at 0.5 V), but also drastically reduces static power due to its lower leakage current.

Table 1: Comparative analysis of stacking effect SRAM cell with existing technologies

Parameter	Stacking Effect (32nm)	45nm Technology	90nm Technology
Width	100nm	110nm	125nm
Supply Voltage	1V	1.1V	1.2V
VDD	1V	1.1V	1.2V
Total SNM	500mV	348mV	305mV
Total Power	173nW	3.1uW	3.5uW

A comparison between three distinct CMOS technology nodes—32nm (with stacking effect), 45nm, and 90nm—for a 6T SRAM cell is shown in Table 1. Important factors including transistor width, supply voltage (VDD), static noise margin (SNM), and overall power usage are highlighted in the comparison. With a standard supply voltage of 1V, the transistor width is decreased to 100nm in the 32nm technology node using the stacking effect technique. With an extremely low total power consumption of 173nW, this arrangement demonstrates its energy efficiency and produces a much higher total SNM of 500mV, suggesting improved stability against noise.

The CMOS width increases marginally to 110 nm at the 45 nm node, with a corresponding VDD of 1.1V. However, this results in a higher power consumption of 3.1µW and a lower SNM of 348mV, suggesting a trade-off between energy efficiency and device scaling.

The VDD is increased to 1.2V and the transistor width is further expanded to 125nm for the 90nm technology node. This leads to the highest power usage (3.5µW) and the lowest SNM (305mV) of the three.

Overall, the findings show that the 32nm SRAM cell with the stacking effect is better suited for low-power and high-performance applications in contemporary VLSI systems since it significantly lowers power consumption while simultaneously improving noise immunity.

VI. FUTURE SCOPE

Even though the current work shows encouraging results, future research can go in a number of areas to further optimize the performance of SRAM cells:

1. *Technology Scaling Beyond 32nm:* To evaluate scalability and quantum effects, the SRAM cell can be implemented and evaluated in FinFET and GAA-based technologies that are 22nm, 16nm, or even 7nm.
2. *Advanced SRAM Topologies:* Developing and evaluating alternative SRAM cell types, such as 7T, 8T, or 10T cells, to improve soft error tolerance, leakage control, and read/write stability.
3. *Process Variation Analysis:* Analyzing how process, voltage, and temperature (PVT) changes affect SRAM performance by statistical simulations (such as Monte Carlo).
4. *Layout-Level Optimization:* Using post-layout simulations and layout design to investigate area, routing complexity, and parasitic effects.

VII. CONCLUSION

The performance of 6T SRAM cells at three different technological nodes—32nm (using the stacking effect), 45nm, and 90nm—is compared in this study. The evaluation of overall power consumption and Static Noise Margin (SNM), which are essential for memory circuit efficiency and dependability, was the main focus.

The findings show that noise immunity and power efficiency are significantly increased by the 32nm technology with the stacking effect. In particular, the SNM outperformed the traditional 45nm and 90nm designs, improving to 500mV and consuming 173nW less power. This demonstrates how sophisticated scaling strategies, like transistor stacking, can lessen the drawbacks of aggressive technological scaling, especially instability and leakage in SRAM cells.

As a result, the suggested 32nm stacking-based SRAM design is ideal for high-speed, low-power applications like cache memories in contemporary processors, portable electronics, and embedded systems.

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