Design of 28GHz Cascode Class E Power amplifier With Class D Driver Circuit for 5G Applications

[#1]Puneeth S, [#2]Rangaraju H G, [#3]Kusuma M S
[#1] Research Scholar, Dept. of ECE, SKSJTI, K R Circle, Bengaluru, Affiliated to VTU, Belagavi
[#2] Dept. of ECE, K R Pet Krishna Government Engineering College, KR Pete, Affiliated to VTU, Belagavi
[#3] Dept. of ECE, Dept. of ECE, GSKSJTI, K R Circle, Bengaluru, Affiliated to VTU, Belagavi

Abstract

The 28-GHz Class E mode power amplifier designed for next generation(5-G) wireless transmission applications at base station using FET technology is described in this paper. To lessen device load class-E as an amplifier, the suggested PA uses the cascode topology. To achieve sharp switching at the power stage of class-E, a class-D amplifier is employed as driver in cascade with Class E power amplifier. Using supply voltage of 17V and a 50 Ω load, the PA provides 16.4 dBm of output power and 35.4% power-added efficiency, according to the simulation results.

Keywords: Power Amplifier, Class-E, Class-D, Cascode, Power- Added Efficiency, S-Parameters, Drain Efficiency

Classification: Integrated circuits

Introduction

High frequencies between ranges of 6 to 100GHz are used as carrier frequency to obtain wider bandwidths in modulation technique and use of number of antennas per transmitter, next generation 5-G communication systems will offer noticeably higher data rates and lower latency. Research for 5G systems at various frequency bands greater than 28 GHz [1] are going on leading to high efficiency power transmitter [7].

The level of power needed for each antenna element in a huge MIMO transmitter decreases as the number of antennas increases. Peak power levels required to power base-station antennas operating at 15 GHz are thought to be between 20 and 27 dBm. High efficiency, linearity, co-integration with other RF front-end circuits, and affordability are further critical criteria for power amplifiers.

High efficiency at high frequencies is provided by SokaI's switching-mode tuned power amplifier, which is depicted in figure 1. A single pole switch device, operating at the output signal's carrier frequency and a network load that has to extract just one spectrum frequency component make up the basic configuration for a class E mode power amplifier. The load network is made up of a series resonant output circuit and a capacitor that shunts the switch device.

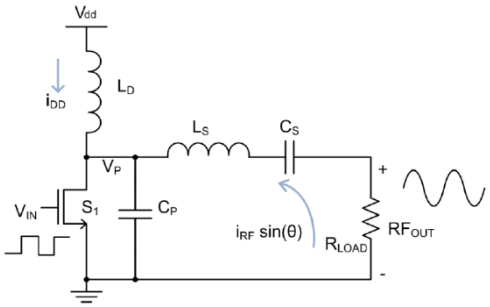

Figure1: Class E tuned power amplifier

Large transistors and inductors used in design of such amplifier will results in lower efficiency and higher power consumption simultaneously. In contrast to `SiGe, GaAs, `BiCMOS and GaN technology, the majority of PA designers now favor CMOS technology [2]. Because the power amplifier able to achieve highest (100%) drain efficiency (DE), researchers are increasingly choosing it for PA design. Class E PA is more efficient and has simpler circuitry than class D and class F PA, which are other switched type PA classes. In contrast to linear amplifiers, switched type amplifiers have the potential in increasing PAE [7]. Because the current and voltage waveforms are shaped such that they do not overlap and allows to achieve great efficiency [8]. Therefore, a well-designed PA [3] is necessary to meet the high demands of narrow band low power, increased battery life, and increased efficiency.

Designing a power amplifier with enhanced properties for millimetre (5-G) wave applications at 28 GHz is the aim of this research work. The suggested power amplifier has a two-stage of design and a cascode class E configuration to reduce power loss and to boost the efficiency.

Why Cascode?

In the basic class-E PA, gate oxide breakdown may result from the high voltage differential across the drain and gate. Since the transistor will be damaged during typical usage cycles, this effect could seriously impair the circuit's long-term performance. Lowering the voltage at the transistor's drain is one way to increase circuit dependability. VDD can be decreased since the link between VP and VDD is completely linear. Nevertheless, POUT is decreased as a result. It is possible to use a cascode architecture in place of losing POUT.

Class-E PA as Cascode topology

The non-cascode variant and the ideal cascode class-E PA operation are extremely comparable. For simplicity's sake, CP is thought to be the parasitic capacitances from M2 combined into a general capacitor, while M1 and M2 are thought to be perfect switches. As seen in figure 1, the rest of the circuit is identical to that of the non-cascode type of PA.

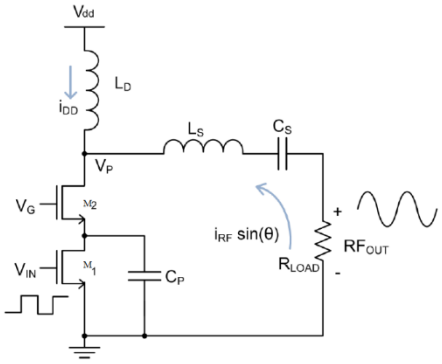

Figure2: Cascode class-E Power Amplifier

Proposed Power Amplifier

Figure 3 displays the proposed class-E PA's schematic. The driver stage and the power stage are the two stages into which the intended PA can be separated. The class-D amplifier is used in the driver stage. The class-D amplifier's input DC voltage is biased toward the output DC values depicted in Figure 3. When compared to a bias technique using division resistors, this feedback resistor can lower DC current consumption and give the class-D amplifiers a steady DC bias voltage [4]. To achieve the desired power gain with the least amount of power consumption, the driver stage must be optimized at 28 GHz.

An inter-stage matching network connects the driver stage and the class-E stage to one another. Due to the class-E stage's input capacitance, the network must incorporate some inductors. However, at 27 GHz, an inductor has a greater loss than at the frequency used by traditional class-E PAs. As a result, it is necessary to reduce the number of inductors. A parallel L and C inter-stage matching network was employed. The greatest PAE at 28 GHz is achieved by optimizing the shunt inductor and capacitor.

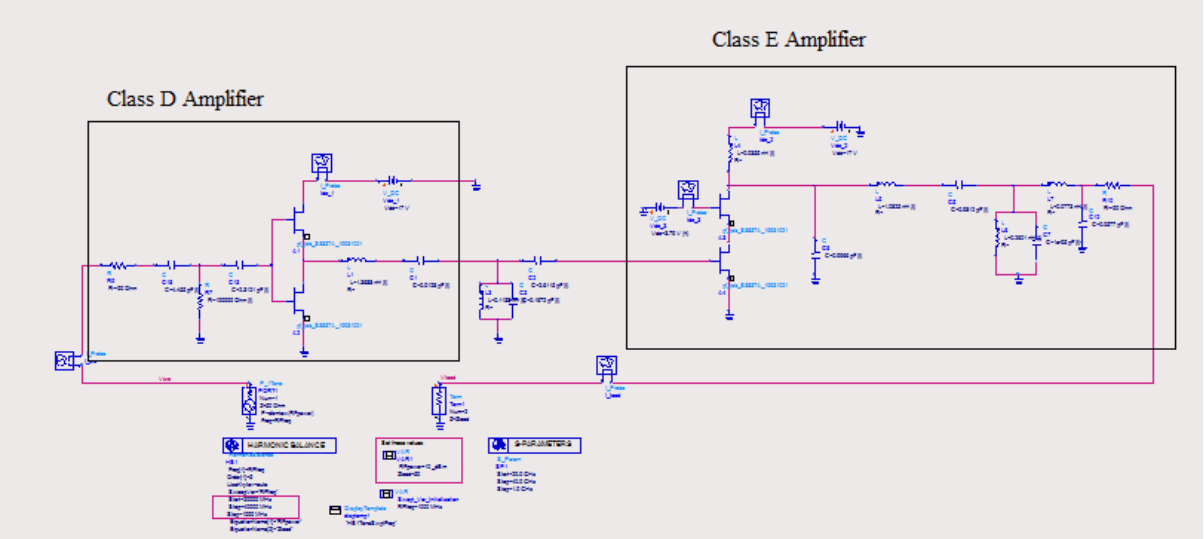

Figure3: Proposed cascade Class E Power Amplifier with Class D Amplifier as Bias circuit

Simulation Results

The ADS tool is used to simulate at 28.0 GHz using bias voltages of 17 V, 17 V, and 3.19 V at Vdd1, Vdd2, and Vb respectively. As can be seen, the recommended PA has a drain efficiency of 38.55%, a PAE of 38.521%, and a maximum output power of 20.21 dBm. Due to the contact resistances effect of the DC probes, the simulation results decreases with total input power. Additionally negative feedback caused due to the parasitic inductance at the source of the CS MOSFET reduces the power gain and PAE.

The figure 4 displays the simulated forward transmission coefficient S21, which is 13.404 dBm, and the reverse transmission coefficient S12, which is -13.283. Figure 4 also shows the `input reflection coefficient S11, which is -10.782dBm, and the `output reflection `coefficient S22, which is -12.311dBm. It is discovered that the VSWR is 2 and the Rollett stability factor is 1.5, both of which are more than 1.

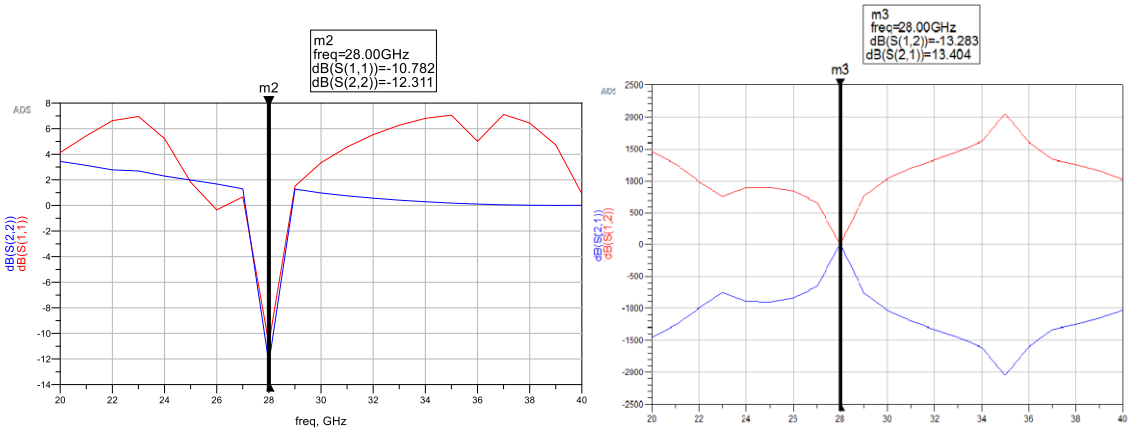

Figure 4: Input (S11) and Output (S22) `Reflection Coefficient, Forward (`S21) and Reverse (`S12) `Transmission Coefficient

The Load Current and Voltage is shown in figure 5. Proposed work compared with previous work is tabulated as below table1.

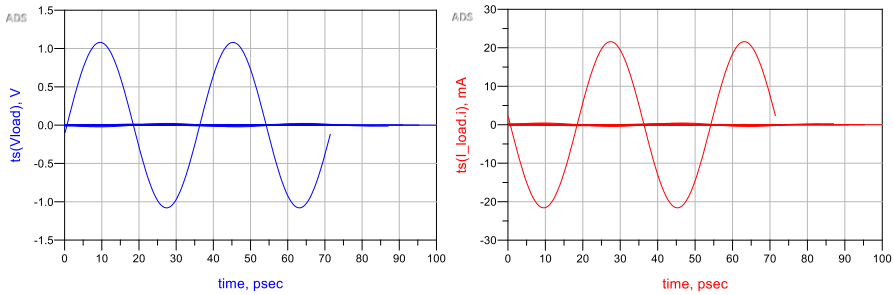

Figure 5: Voltage (Vload) and Current (Iload in mA) at 50Ω load

Table1: Comparison with Previous Works

Ref	Frequency	Psat (dBm)	PAE %	DE%	Class of Operation
This Work	28GHz	20.21	38.521	38.55	Class E Cascode with Class D as Driver
10	28GHz	13	28		Class E Cascode
10	28GHz	13	35	45	Class E switched Cascode
9	28GHZ	28.5	38		Stacked FET

Conclusion

This Paper presents design and measurement of cascode `Class E power amplifier in cascade with Class D Power amplifier as driver circuit at 28GHz using Toshiba packaged FET available in ADS. This proposed topology achieve a power added efficiency of 38.521% and Drain efficiency of 38.55% with saturated output power of 20.21dBm

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