Design of Low Power, Area Efficient 4-bit Magnitude Comparator Using GDI logic

1st Aditya Manjunatha
Electronics and Communication
RV College of Engineering
Bengaluru, India

2nd Shrinidhi Udupa
Electronics and Communication
RV College of Engineering
Bengaluru, India

3rd Dr B S Kariyappa
Electronics and Communication
RV College of Engineering
Bengaluru, India

***Abstract*—This paper introduces a distinct design for the 4-bit Magnitude Comparator, which is used to compare two binary numbers for arithmetic and logical operations in a processor. The GDI logic technique employed in the proposed design ensures low power consumption and efficient area utilization. The algorithm of the GDI logic involves 2's complement addition, facilitating comparison and subtraction of inputs. Depending on the remainder, it determines the relationship between the inputs. The 4-bit Magnitude Comparator designed using conventional CMOS technique comprises 166 transistors. However, in the proposed design, the transistor count is reduced to 62, resulting in decreased power consumption and area utilization. Post-layout analysis reveals approximately 11.60% reduction in power consumption and approximately 13.95% reduction in area utilization with GDI logic compared to conventional logic through comprehensive simulations and performance evaluations, this paper demonstrates the tangible benefits of adopting GDI logic in the design of essential arithmetic and logical units within processors. By reducing power consumption and area utilization while maintaining performance metrics, the proposed design paves the way for more energy-efficient and compact computing systems**

***Index Terms*—Magnitude Comparator, GDI logic, Low Power, Area Utilization**

I. Introduction

A comparator is a device that evaluates two numbers, usually holding one constant while the other changes. The power consumption by the comparator will affect the device performance. The power consumed is classified mainly into two types namely static and dynamic. To minimize power dissipation in VLSI design, several strategies can be employed. Reducing the supply voltage is an effective approach, potentially cutting power consumption by a factor of four with a two-fold reduction in voltage, though performance may be impacted unless threshold voltage is scaled accordingly [1]. Additionally, lowering physical capacitance is crucial, as dynamic power consumption depends on the capacitance being switched. Furthermore, optimization across multiple design process levels from system and algorithmic to circuit and layout can enhance low power VLSI design.

One way to reduce the power consumption is by using a different arrangement of the transistors which will give the same functionality but with reduced power [2]. Gate Diffusion Input (GDI) is one of those methods. Decreasing voltage can be an efficient means of lowering power consumption[3][4]. The size of an integrated circuit (IC) is directly proportional to the number of transistors it contains. Comparator is widely used in CPU, Microcontroller, Combinational and communication systems [5]. The size of an integrated circuit (IC) is directly proportional to the number of transistors it contains. As the number of transistors increases, the physical area of the IC generally increases as well, assuming that the transistor density remains unchanged.

II. conventional cmos design of 4-bit comparator

The conventional algorithm of an N-bit comparator operates by comparing two numbers beginning from the most significant bit (MSB). When comparing the MSB of two numbers, if one is greater than the other, it can be inferred that one number is greater overall. If the MSBs are equal, the comparison proceeds to the next higher bit, repeating the process [6]. This method entails comparing the bits from MSB to least significant bit (LSB). These comparisons adhere to specific conditions outlined in equations (1), (2), and (3). By starting with the MSB, the algorithm effectively reduces the number of comparisons needed, as a significant difference at any higher bit immediately determines the result, bypassing the need to compare the remaining lower bits [7][8]. Additionally, this method leverages a hierarchical decision-making process, where each bit comparison provides a progressively narrower range of potential outcomes, ensuring an efficient and structured approach to determining the overall relationship between the two numbers. This structured comparison ensures that the algorithm operates with a clear and logical flow, minimizing computational complexity and enhancing performance, especially for larger bit-width numbers where the benefits of early termination of comparisons become more pronounced.

$$A_{\mathrm{eq}_B} = (A3 \odot B3)(A2 \odot B2)(A1 \odot B1)(A0 \odot B0) \quad (1)$$

(1)

$$A_{\mathrm{gt}_B} = (A3 \odot B3)(A2 \odot B2)(A1 \odot B1)A0B0' + (A3 \odot B3)(A2 \odot B2)A1B1' + (A3 \odot B3)A2B2' + A3B3' \quad (2)$$

$$A_{\mathrm{lt}_B} = (A3 \odot B3)(A2 \odot B2)(A1 \odot B1)A0'B0 + (A3 \odot B3)(A2 \odot B2)A1'B1 + (A3 \odot B3)A2'B2 + A3'B3 \quad (3)$$

TABLE I
TRUTH TABLE FOR 4-BIT MAGNITUDE COMPARATOR

Comparing Inputs				Output		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	H	L	L
A3 = B3	A2 < B2	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

The truth table presented in Table 1 for the 4-bit comparator delineates the specific conditions for the outputs corresponding to A > B, A < B, and A = B. High voltage level (H) and low voltage level (L) are employed to signify the output states. The comparator initiates the evaluation with the most significant bits (A3, B3) and proceeds sequentially to the least significant bits (A0, B0). For instance, when A3 > B3, the output A > B is set to high (H), while A < B and A = B are set to low (L), regardless of the values of the subsequent bits (indicated by X, denoting "don't care"). Conversely, if A3 = B3, the comparison continues with the next significant bits (A2, B2), and this process persists until all bits have been evaluated. This method ensures a precise determination of whether A is greater than, less than, or equal to B[9].

The Figure 1 illustrates the schematic of a four-bit magnitude comparator. Figure 2 presents the timing diagram for a four-bit magnitude comparator, illustrating the transitions and interactions of the comparator's outputs over a range of input conditions. The waveforms depict the states of the input bits (A3 to A0 and B3 to B0) and the corresponding outputs (A¿B, A=B, and A¡B) over time.

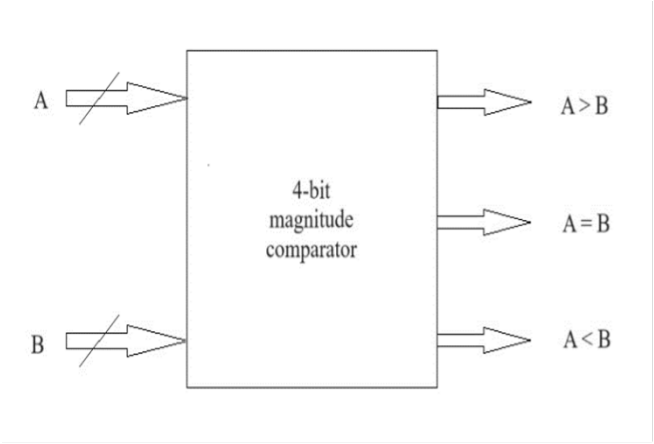

Fig. 1. Conventional design of 4-bit comparator

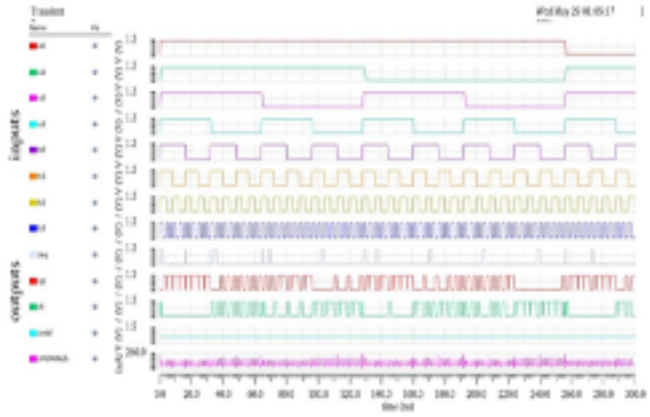

Fig. 2. Output waveform of conventional 4-bit comparator

III. GDI DESIGN OF 4-BIT COMPARATOR

The Gate Diffusion Input (GDI) technique in VLSI design introduces a unique approach to logic gate construction by using three inputs instead of two, differentiating it from standard CMOS inverters [10]. In a GDI cell, when the gate input is at a logic low (0), the PMOS transistor is activated, connecting the output to the source of the PMOS transistor, while the NMOS transistor remains off. Similarly, when the gate input is at a logic high (1), the NMOS transistor is activated, connecting the output to the source of the NMOS transistor, and the PMOS transistor is off. This input configuration enables the implementation of different logic functions [10][3]. The flexibility of the GDI technique allows for the efficient realization of logic gates by appropriate input connections and adding necessary inverters at the output [11].

The algorithm of the GDI logic design uses 2's complement addition. One input is compared with the other and then the difference is calculated[12]. If the remainder is positive, then A is bigger than B. If the remainder is negative, then A is smaller than B. If the remainder is zero, then A equals

B [13]. Compared to conventional CMOS logic, GDI cells can implement various logic functions utilizing only two transistors. This translates to a reduced circuit footprint and potentially lower manufacturing costs. Additionally, GDI logic typically shows lower power consumption because of its efficient use of transistors, making it especially appealing for battery-powered applications. Figure 3 represents the circuit schematic of the 4-bit comparator using a full adder with GDI logic. Figure 4 represents the design of a full adder using GDI logic [14] which reduces the transistor count to 10.

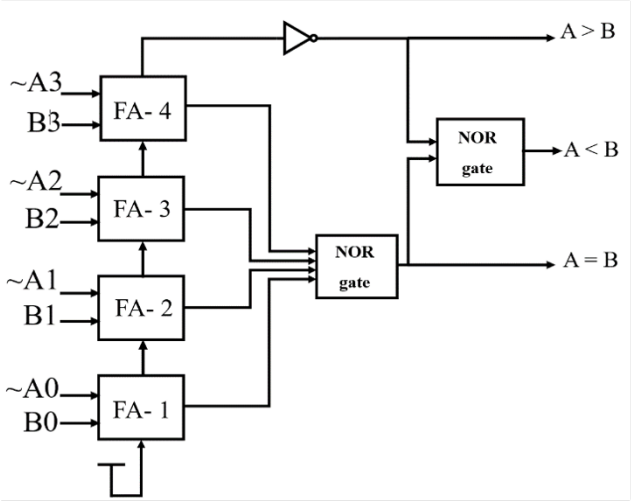

Fig. 3. GDI design of 4-bit comparator

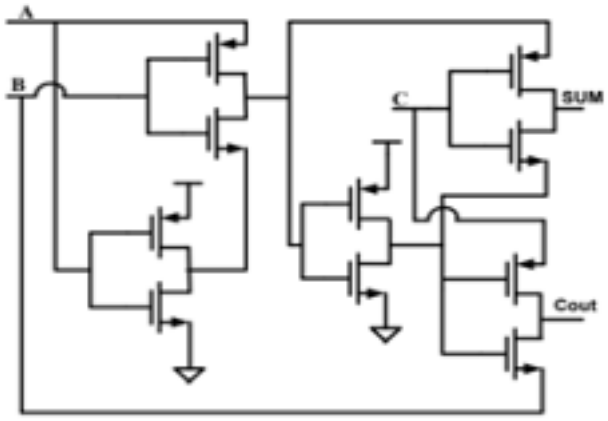

Fig. 4. GDI design of full adder

IV. Results

The proposed 4-bit magnitude comparator using Gate Diffusion Input (GDI) logic shows substantial improvements in power efficiency and area reduction compared to conventional CMOS-based designs. The following subsections provide an in-depth analysis of these results, discussing power consumption, area utilization, performance metrics, and practical implications.

A. Power Usage Analysis

The power consumption metrics were extracted through both prelayout and postlayout simulations across different supplies of voltage ranges from 0V to 1.4V. During the prelayout phase, it reports on Table 2 that the GDI design has immense RMS power reduction at low voltage supplies, though there is a minor increase in middle-range voltage supplies due to fewer transistor counts. Consequently, this trend shows that the low-power design of the GDI logic is particularly favorable under low-voltage conditions, since that would make it all the more suitable for energy-sensitive applications such as portable and/or battery-operated devices. Pre-Layout Analysis vs. Post-Layout: Figure 5 shows the comparative graph for the prelayout power consumption, while Figure 6 presents the postlayout power results at 0.8V, pointing out the continuing power advantage of the GDI design. Such a postlayout analysis presents an 11.60These results are further strengthened by simulations using the OpenROAD tool with the 7nm ASAP7 technology node to ensure realistic assessment and scalability for advanced VLSI implementations.

B. Die Area and Transistor Count

The proposed GDI comparator architecture reduces one of the keys to high-density integrated circuit area utilization by 13.95% Table 3 summarizes the comparison of all these areas for CMOS and GDI-based designs. In addition, the GDI logic circuit consists of only 62 transistors compared to the 166 transistors in a conventional CMOS comparator, thereby making it more compact. This minimum transistor count helps not only in area reduction but also reduces the manufacturing cost and thermal effects, which becomes very important in high-density VLSI systems where dissipation of heat is difficult.

The Figure 7 represents the physical layout of an integrated circuit designed using the Open ROAD VLSI tool. The layout includes various metal layers, vias, and transistor structures. The red, blue, and green lines denote different metal layers used for interconnections, with vias shown as the small rectangles connecting these layers. The overall structure is compact, indicating efficient use of space and adherence to design rules. The scale bar in the bottom left corner, marked in nanometers, shows the design's dimensions, illustrating the small scale typical of modern integrated circuits. This layout represents a critical block of the IC, optimized for performance and area within the constraints of the design specifications.

C. Performance Measures

While the GDI design has focused on the optimization of power and area, some marginal speed trade-off does result from such a simplified structure. The time slack for GDI logic is slightly less when compared to the slack time of a CMOS design, standing at 450.5 ns versus 471.81 ns, respectively.

In this regard, it will turn out to be pretty minor trade-offs in speed, considering those areas where power consumption and compactness are more important than maximal processing speed. These latter great power and area advantages outweigh the marginal speed difference of GDI, therefore; it is a practical choice for applications where efficiency is more valuable than speed, such as embedded systems and portable electronics.

D. Practical Advantages and Application Scope

In particular, the proposed GDI-based comparator design is beneficial in this environment where power efficiency, compactness, and thermal management are required. Due to area and power reduction, it is highly recommended in battery-powered applications and for environments where stringent power budgets are required.

1) Portable Devices: GDI comparators are hence appropriate for portable electronics, as that uses less power and area. The lesser the power used; the longer the battery life, which is one of the most critical factors for customer satisfaction with portable electronics.

2) Wearable and IoT Applications: GDI design enables small form factor and best energy efficiency in IoT and wearable applications, due to the higher density of integrated circuits that can fit within the limited space. The phenomenon of low power feed kp reduces thermal generation, which in turn furthers the case for compact and enclosed spaces, as with wearable devices.

3) Edge Devices Data Processing Units: It requires low-power, compact components to process data efficiently with limited energy. GDI-based comparators can improve performance within an edge device, which is suitable for real-time processing without any power availability.

TABLE II
TABLE REPRESENTING COMPARISON OF POWER IN PRE LAYOUT

Supply Voltage, Vdd (V)	Conventional design RMS Power (in micro watt)	GDI logic design RMS Power (in micro watt)
0	0	0
0.2	0.76	0.5269
0.4	7.692	9.262
0.6	4.336	6.53
0.8	9.534	14.07
1.0	17.106	8.866
1.2	28.819	15.42

TABLE III
COMPARISON ON THE TWO DESIGNS BASED ON DIFFERENT PARAMETERS

Parameters	Conventional [5]	GDI logic
Area Utilization ($1\mu m^2$)	43%	37%
Slack (in ns)	471.81	450.5
Number of transistors count	166	62

CONCLUSION

The 4-bit Magnitude Comparator built using the conventional CMOS technique consists of 166 transistors. However,

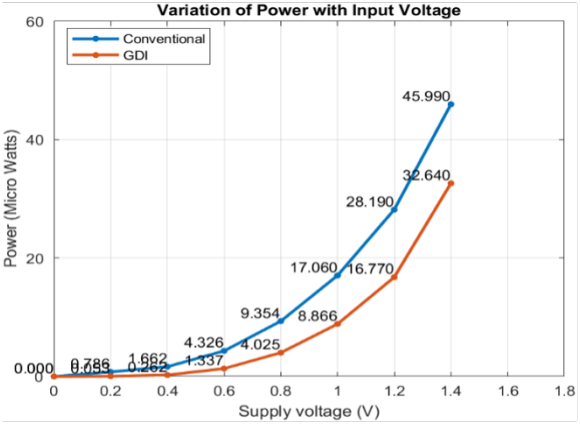

Fig. 5. Graph for the pre layout simulation

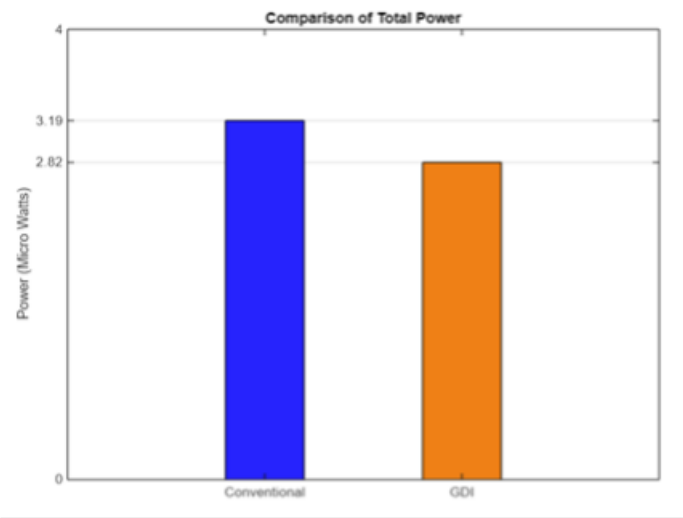

Fig. 6. Graph for the post layout simulation for the two designs

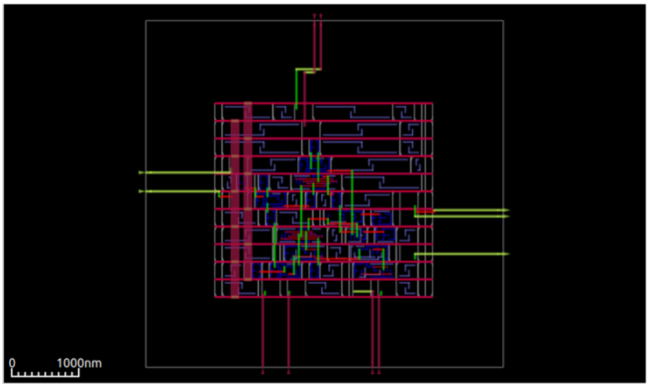

Fig. 7. The physical layout for the proposed design using OpenROAD tool

in the proposed design, the transistor count has been reduced to 62, which represents a decrease of approximately 62.65%. This reduction also leads to lower power consumption and a smaller area. The power is reduced by approximately 11.60% in the GDI logic compared to the conventional value in post layout. The area utilization is reduced by approximately 13.95% in GDI logic compared to conventional logic in post layout analysis. While GDI logic often features simpler circuitry compared to more sophisticated CMOS designs, it's important to note that the streamlined approach may sacrifice some level of flexibility in certain scenarios. The GDI based logic can be used in circuit design for its advantages in reducing power consumption and area making it suitable for applications such as arithmetic circuits, memory cells, and power management. It enables efficient implementation of basic logic gates, multiplexers, flip-flops, and ADC/DAC circuits.

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