Design and Analysis of 3- stage Current Starved Ring Oscillator for EEPROM

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Abstract: **The recent developments focus on low power high, speed designs for portability. This paper presents a new technique design of a three-stage single-ended current-starved ring oscillator (CSRO) to improve frequency performance of CMOS ring oscillator It is based on the addition of MOS transistor to boost switching speed of the oscillator delay cell using *Cadence Virtuoso*, *in GPDK* 90*nm technology.* A current-starved ring oscillator (CSRO) is a voltage-controlled oscillator (VCO) that uses a control voltage to limit the current available to the inverter. The oscillator achieves a tunable frequency range of 20 MHz to 100 MHz by varying the control voltage Vctrl.**

Keywords: CMOS, CADENCE Virtuoso, Current Starved Ring Oscillator

1. INTRODUCTION

Low power Ring oscillator (RO) are the main constructive block of the VLSI circuit systems which are used ROs are used as VCOs in phase-locked loops (PLLs) for clock synthesis and frequency modulation, in EEPROMs by generating internal clock signals.

A Voltage controlled oscillator (VCO) is one of the important, basic building blocks in analog and digital circuits. Voltage controlled oscillator, or generally oscillator, is a key element in a lot of electronics systems such a frequency synthesizer, PLL and telecommunication systems.

Many works have reported for low power ring oscillator design using CMOS inverter, current starved (CS) inverter technique to have more delay which in turns decrease frequency and power efficiently. The delay of inverter is increased using various method like voltage scaling, transmission gate, and inverted inverter. These inverter design techniques can be used to generate lower frequency of oscillation with low power consumption.

A current-starved oscillator is a type of voltage-controlled oscillator (VCO) where the current supplied to the oscillator stages is limited or "starved" by additional transistors. This design allows for finer control over the oscillation frequency and power consumption. The current-starved approach includes biasing the transistors with a continuous current source to reduce their operational current. A control voltage (Vctrl) is supplied to the ring oscillator to enable it to function as a VCO.

2. RING OSCILLATOR CIRCUIT

2.1 Ring Oscillator

Ring oscillators are fundamental building blocks in both digital and analog circuits. A ring oscillator consists of an odd number of inverting amplifier stages with feedback to its input (Fig.1). When the input voltage is applied to the first stage, an odd number of stages produces an inverted output, causing oscillation to begin. If the circuit contains an even number of inverters, it cannot function as a ring oscillator, as the output of the last stage will be the same as the input of the circuit.

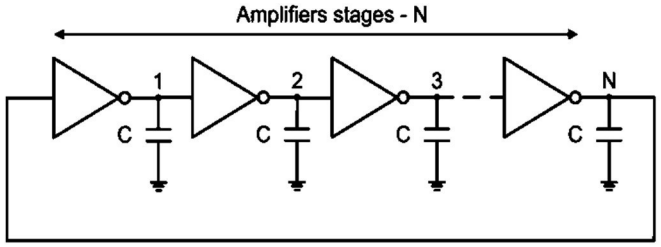

Fig. 1. N-stage ring oscillator

Ring oscillators generate timing signals for synchronous operation and are frequently used as clock generators in digital systems. They can also serve as frequency dividers, separating higher frequencies into lower ones. Two primary types of oscillators are used in digital system design: the LC tank oscillator and the CMOS ring oscillator.

Compared to LC tank-based oscillators, CMOS ring oscillators offer several advantages, including a smaller size, higher integration, lower operating voltage, and a wider oscillation range. Due to their low power dissipation and high synthesizability, n- stage CMOS ring oscillators find a wide range of applications, such as modulation, demodulation, SRAM, and high-speed input-output modules.

The oscillation frequency of a ring oscillator is represented as

$$f_{osc} = \frac{1}{2nT_n},$$

where, n= no. of inverter stages $T_{n=}$ time delay of inverter

2.2 CMOS Circuit

A CMOS inverter is a basic building block in digital electronics, particularly in complementary metal- oxide-semiconductor (CMOS) technology. It is a logic gate that implements the NOT function, meaning it inverts the input signal In CMOS ring oscillator the inverting stage or the inverter is a circuit which is built from a pair of nMOS and pMOS transistors operating as complementary switches (Fig.3)

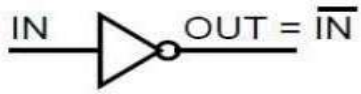

Fig. 2. Inverter Symbol

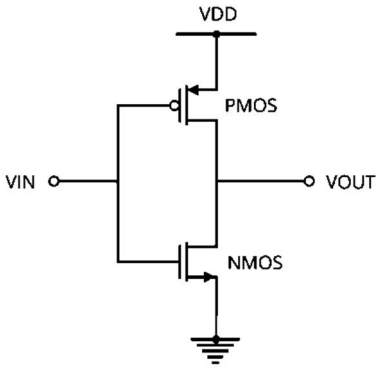

Fig. 3. CMOS Inverter stage

CMOS inverters consume very little power when they are in a steady state, whether at logic 0 or logic 1, because one of the transistors is always off. Power is mainly used during the transition between these states, which occurs for a brief moment when both transistors conduct simultaneously, resulting in a short spike in current.

CMOS inverters exhibit significant noise margins, reflecting their ability to tolerate noise at both high and low logic levels, which is determined by the voltage transfer characteristic (VTC) that indicates the noise tolerability without impacting logic states.

3-PROPOSED DESIGN

The key aspect of this arrangement is that it should consume less power and exhibit minimal variation in movement frequency in relation to temperature.

Therefore, the setup consists of a series of current-starved inverters combined with a temperature-compensating biasing circuit. The design so implemented allows for finer control over the performance parameters such as frequency of oscillation and power consumption.

3.1 Current Starved oscillator

The current-starved oscillator is a kind of voltage- controlled oscillator (VCO) where the current supplied to the oscillator is limited or 'starved' by addition of transistors. The current-starved approach includes biasing the transistors with a continuous current source to reduce their operational current (Fig.4). A control voltage (Vctrl) is supplied to the ring oscillator to enable it to function as a VCO(Fig.5).

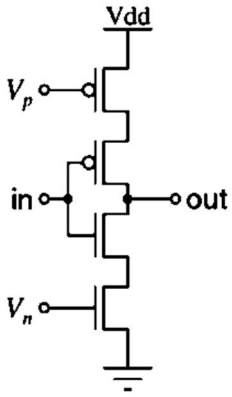

Fig. 4. Single inverting stage of current starved RO

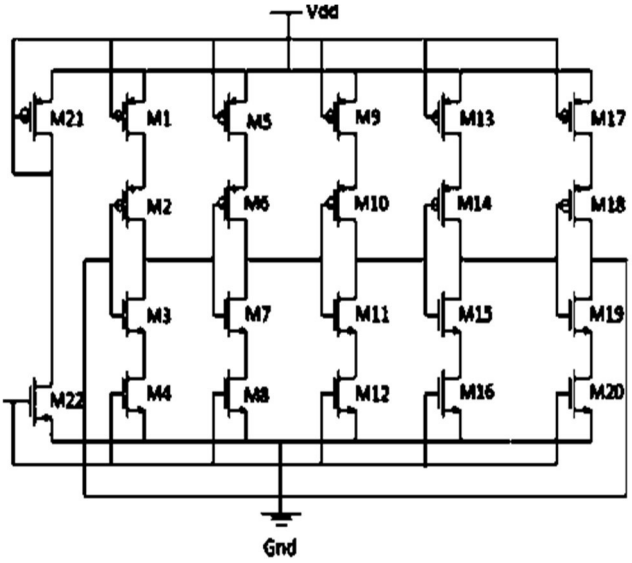

Fig.5. Circuit Diagram of current starved VCO

3.2 How does it work?

In order to control the oscillation frequency, the current through the transistors is starved using additional transistors & current sources.

This is done by placing a series of transistors in the direction of flow of the current, efficiently limiting the amount of current that can flow through the individual inverters.

To control the frequency of the oscillation we can adjust the amount of current starvation by changing the biasing current, the delay through each inverter stage can be varied, which in return changes the frequency of the oscillation.

The gate terminal of these starving transistors is connected to a controlled voltage (Vctrl). By adjusting Vctrl, we can regulate the amount of current that these transistors will allow to pass through the inverters.

3.3 Advantages over Traditional Ring Oscillator

Power Efficiency: Current-starved oscillators consume less power compared to traditional oscillators, making them suitable for low-power application making it ideal for battery-operated and low-power devices.

Frequency Control: Current-starved oscillators offer better control over the oscillation frequency, using additional transistors to limit the current flowing through

the oscillator stages, the oscillation frequency can be finely adjusted.

This is because the frequency of oscillation is directly related to the current supplied to the circuit.

Integration Capability: Current-starved oscillators are easier to integrate into CMOS technology, leading to smaller chip area and lower production cost.

Wide Tuning Range: Current-starved oscillators provide a wider tuning range, which is beneficial for applications like phase-locked loops (PLLs) in wireless communication system.

4. SIMULATION RESULT

The proposed CMOS ring oscillator has been simulated using the Cadence Virtuoso tool in a 90 nm technology process. For the NMOS transistors, the width (W) is set to 120 nm and the length (L) is 100 nm, while the PMOS transistors also have a width of 120 nm and a length of 100 nm. The supply voltage for the circuit is 1 V. The schematic of the proposed circuit is shown in (Fig 6)

During the operation of the ring oscillator, when an input is applied to the first inverter, the output of the ring oscillator takes some time to stabilize due to the cascading stages of the circuit. The output waveform of the proposed CMOS ring oscillator at a supply voltage of 1V is observed during this process (Fig. 7).

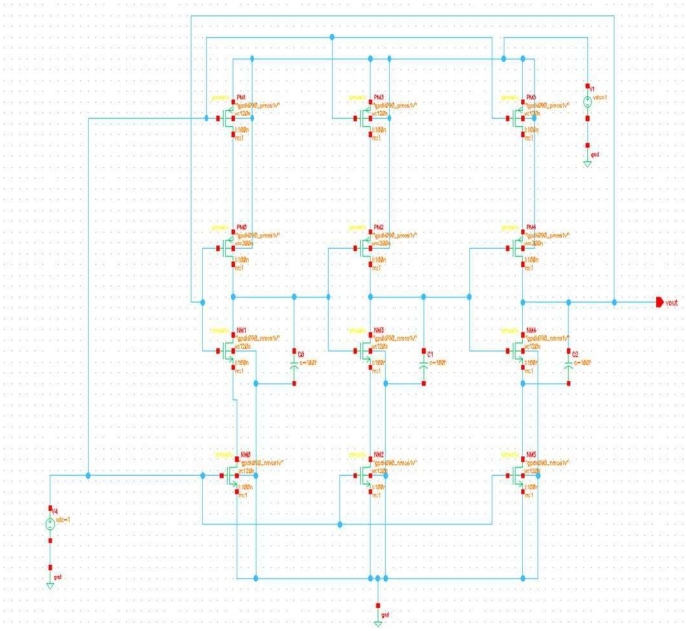

Fig.6. Schematic of 3 stage current starved RO

After simulation, the designed schematic provides a frequency of 1.001 GHz as observed in Fig.7

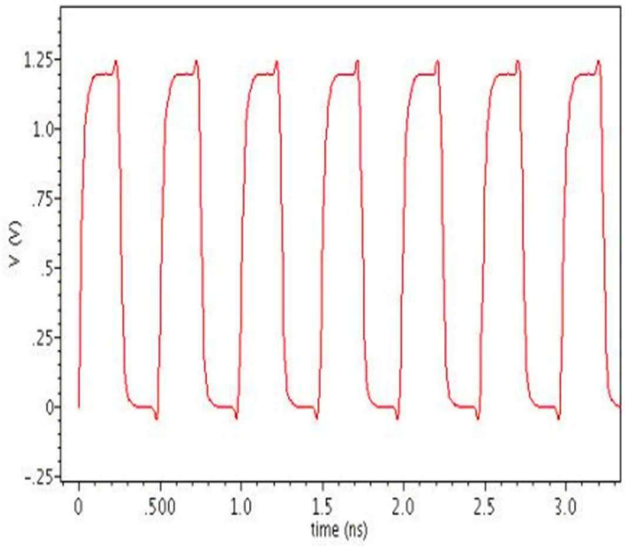

Fig.7. Transient Response of 3 stage current starved RO

PARAMETRIC ANALYSIS:

Parameters	Traditional 3-stage Ring Oscillator	3-stage Current Starved oscillator
Technology	90nm	90nm
Frequency (MHz)	25.02	45.78
Power (µW)	3.584	1.732
Supply Voltage	1 V	1 V

TABLE:1 PARAMETRIC ANALYSIS OF DIFFERENT CIRCUITS

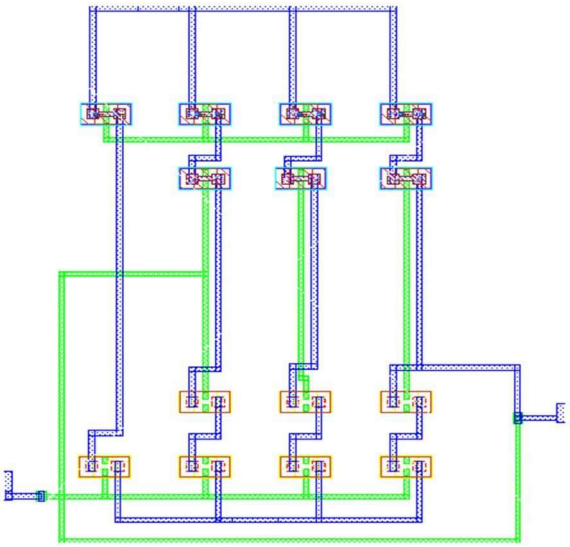

Fig:8 Layout 3-stage current starved VCO

5. CONCLUSION

A current starved ring is simulated to overcome the challenges present in the existing VCO in high-frequency applications. These challenges include leakage current, phase noise, and limited frequency tuning range. To ensure its robust ness, extensive simulations are performed under extreme conditions.

The proposed circuit consumes very less power which is 91 % less than existing circuit due to current starved ring oscillator. It achieves 80.18 % improvement in oscillation frequency because of the current starved voltage supply.

This confirms the robustness of the proposed design, making it a promising solution for high frequency applications. These improvements are achieved at a supply voltage of 1 V.

From the obtained results, it is concluded that the proposed design outperforms existing works in various performance parameters and it is highly suitable for EEPROM applications including wireless communication and radio frequency.

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