PREDICTION IN VLSI LOW POWER CMOS LOGIC CIRCUIT

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Abstract: Microprocessors, digital signal processors (DSPs), and other high-performance digital devices are becoming more and more dependent on low power architecture. High integrated density and increased clock speeds are characteristics shared by these cutting-edge processors. Clock speeds are directly proportional to the power dissipated by chips, which in turn causes temperature increases. Effectively controlling this thermal energy is crucial in order to keep the chip's temperature within acceptable parameters, presenting a notable obstacle. As a result, the expenses related to packaging, cooling, and efficient heat removal increase significantly, becoming important factors to consider in the design and implementation of these circuits. Effective heat management solutions are crucial for ensuring the dependability and durability of high-performance digital systems. Hence, there is a critical requirement for inventive methods in low power design, which is propelling the advancement of materials, topologies, and cooling technologies. This is aimed at reducing the negative effects of power dissipation on both the temperature and financial aspects of high-performance chips.

Keywords: pMOS, CMOS, nMOS, Integrated Circuit, VLSI

Introduction: For the purpose of lowering the amount of power that is lost in digital integrated circuits, the emphasis will be placed on circuit or transistor-level design measures. The quantity of power wasted may be decreased by using various design strategies and power consumption sources. Modern digital circuits made of complementary metal-oxide semiconductors (CMOS) typically have three main power consumption components: dynamic power consumption, short

circuit power consumption, and leakage power consumption. Additionally, ultra-large-scale integration (ULSI) circuit reliability is an important consideration that emphasizes the need of DC design. Digital circuit reliability concerns such as electromigration and hot carrier-induced device deterioration are significantly correlated with peak power dissipation. It is absolutely necessary to find solutions to these problems in order to further improve the functionality and durability of digital integrated circuits.

Levels of Power Consumption

The switching power dissipation is the amount of energy that is lost when a logic transition occurs at the output node of a CMOS logic gate, which is also called a switching event. Dissipation of switching power happens in digital CMOS circuits when charging the output node capacitance draws power from the supply. The voltage at the output node usually goes straight from 0 to VDD as this charging phase goes on. In addition, at this stage, the conducting pMOS transistors lose half of the energy that comes from the power source as heat.

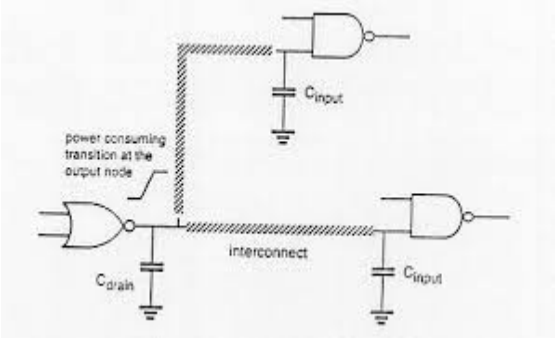

Figure 1: Two NAND gates are driven by a NOR gate via interconnection lines.

$$P_{avg}=\frac{1}{T}\left[\int_{0}^{\frac{T}{2}} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt+\int_{T/2}^{T}\left(V_{DD}-V_{out}\right)\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$

2. Short Circuit Power Dissipation

Charging the parasitic load capacitances inside the circuit accounts for the whole power wasted during switching. And the rising and falling times of the input signals don't influence the switching power in any way. In CMOS inverters or logic gates, both the nMOS and pMOS transistors may briefly conduct during switching if the input voltage waveforms have limited rise and fall durations. Hence, a direct current path exists between the ground and the power source.

When nMOS and pMOS devices flip on, a current known as the short circuit current flows across them. It is not this component that charges the circuit's capacitances. This is more common in cases when the output load capacitance is minimal and the rise and fall durations of the input signal are greater than typical. The following are the power source current components, input and output voltage waveforms, and a symmetrical CMOS inverter operating with a small capacitive load:

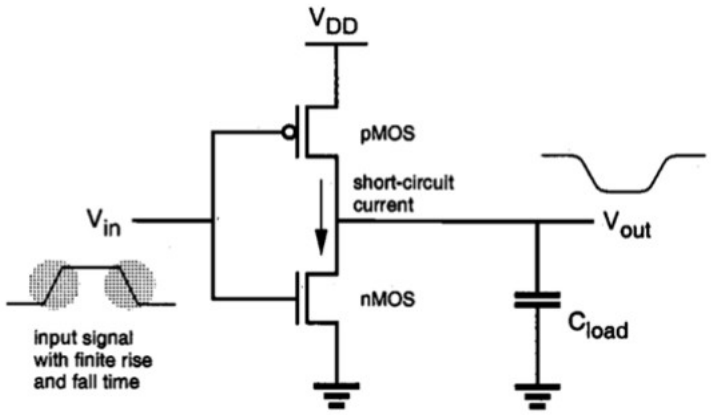

Figure 2: A brief circuit current may be conducted simultaneously by both nMOS and pMOS transistors during switching.

3. Leakage Power Dissipation

Subthreshold currents and reverse leakage that are not zero are generally observed in the nMOS and pMOS transistors that are employed in a CMOS logic gate. Even when the transistors are not

undergoing any switching events, these currents have the potential to contribute to the total power consumption of a CMOS VLSI device with a high number of transistors. The processing parameters are the primary factor that determines the size of the leakage currents inside the system.

When the drain-to-bulk pn-junction of a transistor is biased in the opposite direction, a phenomenon known as reverse diode leakage occurs. There are two primary sources of leakage current in a MOSFET, and this is one of them. The next step is to reverse-bias the power supply connection to the drain in order to extract a current that signals reverse saturation. Consider a CMOS inverter with an active nMOS transistor; the input voltage is high, but the voltage at the output node is zero. Diode leakage at the drain junction may still happen even if the pMOS transistor isn't working well. This is because the drain and n-well have a VDD potential difference in the opposite direction. Likewise, VDD inverts the bias between the pMOS transistor's n-well region and the p-type substrate. That being the case, the n-well junction is responsible for the existence of an additional large leakage current component.

The expression for the reverse leakage current found in a pn-junction is as follows:

$$I_{reverse}=A.J_s\left(e\frac{q\,V_{bias}}{kT}-1\right)$$

At a junction, Vbias represents the reverse bias voltage, Js stands for the reverse saturation current density, and A is the area of the junction. With a typical density of 1–5 picoamperes per square meter, the reverse saturation current density increases significantly with increasing temperature. Even in standby mode, when there is no switching taking place, reverse leakage might nevertheless come about. With a big chip that has several million transistors, the power dissipation that may occur as a result of this process can thus be rather serious.

Examples of Actual Power Dissipation

It is equally crucial to have a complete grasp of how a large-scale system or chip uses electricity. This pattern illustrates the dissipation of power throughout the many components of the semiconductor. Gaining a better grasp of the main components of power consumption in CMOS VLSI chips will help us concentrate our efforts on minimizing power dissipation in large-scale systems and stay on top of the situation. By citing relevant research publications, we may better

understand how to control power in complicated integrated circuits and direct our efforts accordingly.

circuit description	estimated power dissipation (mW)	error wrt circ. sim. (%)	glitch power (%)	vectors needed for confid. interval of		
				25%	10%	5%
inv. string	1.64	-5.7	0	72	>100	>100
parity check	1.28	0.0	56	14	86	>100
booth mult.	18.0	10.4	60	6	17	82
MILL	224	-	8	2	3	7

Table 1: Power Dissipation Analysis Results

Conclusion:

While there are many different factors that contribute to VLSI power consumption, there is just as much variability in the methods used to lower this consumption. Furthermore, some of these approaches are contradictory, meaning that they reduce one form of power consumption while simultaneously raising another type of power consumption. When compared to optimizing power usage on one side, this is a far more difficult job. In light of this, the approach that is used to evaluate power usage is also very important. There are several advantages that may be gained by optimizing the power consumption of integrated circuits. These advantages include an increase in the battery life, a decrease in energy expenditures, a decrease in the amount of heat produced by the device, and a reduction in environmental pollution. Taking into account the cumulative impact of these elements, the evolution of human civilization will also proceed in a more advanced manner. For this reason, it is worthwhile to spend in research and development as well as application.

As a result of the study described above, the following is the conclusion that this article draws: One may distinguish between dynamic power usage and static power consumption when it comes to very large scale integration (VLSI). Based on the operating scale, the methods for reducing these power consumptions can be divided into three categories: transistor-level optimization, gate-level optimization, and system-level optimization. These three categories

correspond to improving the parameters of each transistor, changing the composition and connection of logic gates, and changing the operating mode of the entire system. When it comes to the estimate of power consumption, it is primarily separated into two categories: high-level power consumption estimation and low-level power consumption estimation. The only way to produce a design that satisfies practical needs and reduces overall power consumption is to take into account all of the aspects that contribute to power consumption in a comprehensive manner and to strike a balance between the different ways of power reduction.

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