GBB technique to enhance performance of near threshold circuits

Nalubolu Geetha Rani[1], N.Praveen Kumar[2], Madhusudhana Reddy Barusu[1], D Venkata Srihari Babu[3], Supraja.V[2]

[1]Department of ECE, Ravindra College of Engineering for Women, Kurnool, India
[2]Department of ECE, G. Pullaiah College of Engineering and Technology, Kurnool, India
[3]Department of ECE, G. Pulla Reddy Engineering College, Kurnool, India

ABSTRACT

The demand and the need for low-power electronic circuits is an ever increasing trend particularly for portable battery-operated devices. Various techniques have been employed to reduce both dynamic power and static power consumptions. Recently subthreshold circuit design has become an alternative method for achieving ultra-low power consumption. Circuits operating in this weak inversion region utilize a supply voltage which is less than the threshold voltages of MOS transistors. This low supply voltage operation results in ultra-low-power consumption of the circuit, but with increase in propagation delay of the circuit. In this paper, body bias technique has been employed to enhance performance of subthreshold circuits. Simulation results are done out using cadence software at 45nm technology.

Keywords: Leakage currents, subthreshold conduction, body bias technique.

1. INTRODUCTION

In semiconductor Industry, with rapid growth in development of the digital ICs, power consumption is the considered as the first order design constraint. The power density of the IC increases with small process geometries, high transistor density integration and with higher clock speeds. Scaling is a factor through density of chip can be increased. By scaling, speed of chip can be increased. For technologies below 90nm, leakage power need to be reduced especially for ASIC design process. Exponential rise in the leakage currents takes place due to reduction of supply voltage and threshold voltage at lower geometries. At certain node, leakage power meets dynamic power. Figure 1 shows magnitude of leakage current flow with technology scaling.

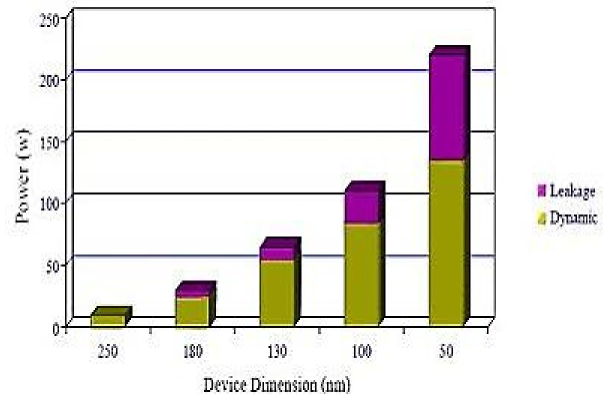

Figure1. Leakage versus Dynamic power with Technology

2. SOURCES OF POWER CONSUMPTIONS

There are majorly three sources of Power consumptions in a CMOS circuit They are

1) Dynamic Power consumption
2) Static (or leakage) power consumption and
3) Short circuit power consumption.

Dynamic (or switching) power consumption takes place due to switching activity. i.e., during charging and discharging of output node capacitance. The currents flowing through transistor in weak inversion region can be considered as leakage current or static current. Short circuit power consumption takes place when both NMOS and PMOS transistors conduct simultaneously for a short amount of time.

Again leakage currents are classified into three major sources they are:

(a) Tunneling Gate oxide tunneling current
(b) Subthreshold leakage current
(c) junction leakage current

(a)Gate oxide tunneling leakage

With supply voltage reduction at Nano regime, the oxide thickness also needs to be scaled. This increases the electric field across the oxide, resulting in tunneling of electrons from gate to body and from body to gate terminal. This results in flow

of undesirable current called leakage current to flow across gate oxide. This is known as fowler Northeim tunneling current. To reduce these leakage currents high-k dielectrics can be used for oxide.

(b)Subthreshold leakage

This leakage current flows through the channel of MOS transistor when the transistor is operating in weak inversion region. i.e., when Vgs is less than Vt. This currents flows due to diffusion of charge carries across the channel. The magnitude of the sub-threshold leakage current is a function of temperature, supply voltage, device size, and process parameters.

(c)Reverse-bias source/drain junction leakages

The drain to body and source to body junctions forms a diode. When diode is in reverse bias condition a small amount of current flows which is nothing but reverse bias leakage current.
The magnitude of this leakage current depends on the area of the source/drain regions and doping concentration.

In addition to above said leakage currents there are leakages due to Gate Induced Drain Leakage (GIDL) and hot carrier injection.

GIDL: This is the phenomenon where gate terminal of MOSFET is grounded and high voltage is applied at the drain terminal. This results in increase of depletion region across gate to drain overlap region.
Gate current due to hot-carrier injection: Due to thin oxide layer at nano scale geometries and high electric fields across the gate terminal, the charge carriers enter from substrate to gate. This is termed as hot carrier injection. Due to this the threshold voltage of the device is altered.

With continuous scaling of MOS device, these leakage currents increase drastically. According to International Technology roadmap for Semiconductors, the power consumed by an IC due to these leakage currents exceeds dynamic power if device is scaled below 45nm. Various techniques like MTCMOS, stacking, SVL technique, input vector control, sleepy stack approach, variable threshold technique, LECTOR technique..etc., have been proposed to reduce these leakage currents. But these techniques can reduce leakages maximum up to 40-55% but not completely. One alternate solution to reduce power consumption of an IC due to these leakages is to utilize these leakage currents for circuit operation. This is called subthreshold conduction.

3. SUB-THRESHOLD CONDUCTION

Sub-threshold conduction or sub-threshold leakage or sub-threshold drain current is the current that flows between drain and source of a MOS transistor when it is in weak-inversion region. i.e., the gate-to-source voltage is less than the threshold voltage of MOSFET. Previously for long channel MOSFETs, the amount of current flowing in sub-threshold region is very small and neglected. Transistor sizes are reduced to nano-scale, this current has become dominant. This current in subthreshold region is considered as leakage current. With technology scaling these leakages current increases and contribute major 50% of total power of a chip. By operating transistors in sub-threshold region, these leakage currents can be used for circuit operation and also power consumption can be reduced. This can be achieved by making supply voltage less the Vt of the transistor. This makes all transistors in the circuit to be operated in sub-threshold region. But, the dis-advantage with this method is increase in delay. So to enhance speed of circuits operating in sub-threshold region, body bias technique is employed.

4. GATE LEVEL BODY BIAS TECHNIQUE

This technique is used to increase speed of IC’s. Here the built-in body bias generator (BBG) circuit produces substrate voltage (V_Bulk) of pull-up and pull-down networks dynamically based on status of logic gates. Voltage signal from the output node is transferred to the substrates of pull-up and pulldown networks to detach body capacitances present at the output. Fast transition is made in the pullup network by sending low voltage on to V_Bulk net through PMOS transistor in BBG circuit when the output node voltage is ‘0’ V. Fast transition in the pull down network is made by sending high voltage on to V_Bulk net through NMOS transistor in BBG circuit when the output node voltage is ‘V_{dd}’ V.

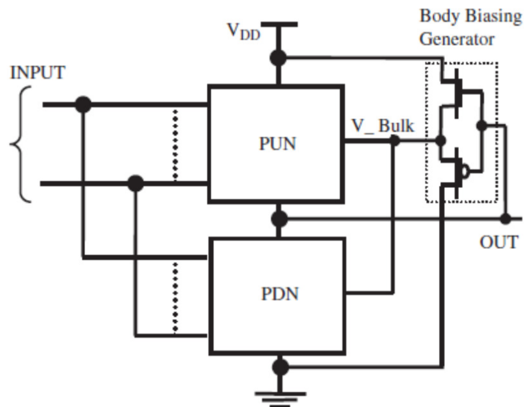

Figure.2 Proposed Technique

5. SIMULATION RESULTS

Simulations are done using cadence tool (Version:IC 6.1.5) at 45nm technology node

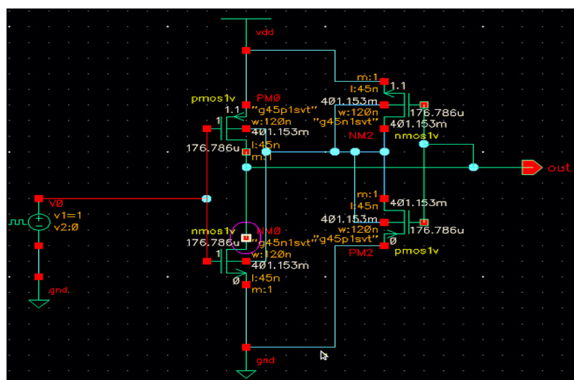

Figure 3. Schematic of sub-threshold Inverter with body bias Technique

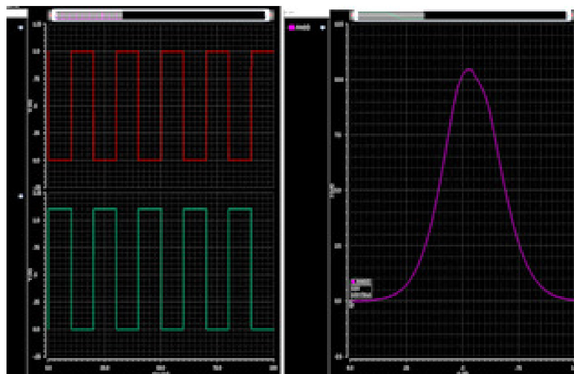

Figure 4. Response of sub-threshold Inverter with body bias Technique

Table 1: Tabulated Results

Supply Voltage	Circuit	Delay	
		Conventional circuits	Body bias Technique
0.3V	Inverter Circuit	51.14001 E-12	24.8 E-14
	NAND gate circuit	68.4102 E-12	31.35 E-14
	NOR gate circuit	61.5002 E-12	34.1 E-14
	6T-SRAM cell	291.056 E-12	187.9 E-14

6. CONCLUSION

Operating circuits in subthreshold region is evolved as an alternative to reduce leakage power for the applications which does not require high speed but low power consumption. To increase performance of circuits, gate level body bias technique is employed. Simulation results show that this technique enhances performance of subthreshold ciruicts.

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