FPGA based Accelerators for ECG signal classifications using Convolutional Neural Network– A Brief Review

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Abstract - Electrocardiogram (ECG) is the recorded form of electrical potential induced by cardiac impulse, measured through the electrodes placed on body surface on opposite sides of the heart. These signals are a vital feature to identify a healthy body. CNN uses a huge amount of data and large number of multiply and accumulate (MAC) operations. Graphical Processing Units (GPU) is proven to be an efficient solution for CNN implementations with huge training dataset but is a computationally expensive solution. In recent times, several Field Programmable Gate Array (FPGA) based solutions are accepted as a choice for CNN implementation. The implementation is likely to demand pipeline structure for synchronization and pooling purpose. Reconfigurable FPGA would allow use of multipliers rather than MAC and hence would provide a better solution for hardware realization. FPGA is certainly a well thought out solution that would additionally facilitate energy efficiency. For applications involving healthcare IoT, FPGA would provide the required flexibility and hence would support IoT device interfacing with outside world with low power, minimal latency and probably best determinism. A limited amount of work has been reported in literature that explores the usage of resource constrained FPGA acceleration for classifying ECG signals via CNN for detecting abnormalities in heart beats. In this investigation, an attempt is made to bring out the state of the art where FPGA acceleration is a potent solution for implementing CNN in identifying/classifying heart diseases and using in such healthcare IoT systems.

Keywords - Electrocardiogram (ECG) classification, FPGA, Convolutional Neural Networks, hardware accelerators, IoT

I INTRODUCTION

In a cardiac cycle that begins with one heartbeat till the next one appears; an action potential is generated spontaneously in the sinus node that travels from the atria (primary pumps) into the ventricles while at the same time pumping blood in to a body's vascular system. Electrocardiogram (ECG) is the signal generated by heart in the form of electrical voltage signal that are recorded from the surface of a body by electrocardiograph. Cardiac arrest is the cessation of all electrical control signals in heart leading to abnormality of cardiac rhythmicity. In an adult abnormal Sinus Rhythms are classified as: "tachycardia", fast heart rate (greater than 100 beats/min) and "bradycardia", slow heart rate (lesser than 60 beats/min) [1].

Electrical signals during heart muscle depolarization triggered via each heartbeat can be measured through ECG. Generally, waveforms recorded through standard 12-electrodes are used in diagnostic centers for detecting abnormalities in the PQRST wave. In the research front, apart from heavy duty, costly biomedical devices, hardware prototypes such as the reported work [2, 3] for Internet of Things (IoT) platform has been highly cited. Field Programmable Gate Arrays (FPGA) has also been widely used as a resource constrained, low-power, parallel processing, higher throughput and low-cost prototype to detect ECG signals and their metrics. This has been used reportedly for features like R-peak heart rate detection, as accelerators for filtering and denoising signals via various algorithmic methodologies, among many others.

A surge in number of cardiovascular patients, lack of skilled medical fraternity and unavailability of proper resources has made the area of automatically detecting and classifying ECG signals of prominent significance, which has been reported since long [4]. Beginning from premature ventricular contractions essential for arrhythmias [5], a number of articles can be found in the literature. For detecting abnormalities via classifying ECG signals using CNN can be found in the literature aplenty as well [6]. But attempting to use FPGA, a resource constrained prototype, as accelerators for ECG signal classifications using CNN is scarcely available. Thus an attempt has been made in this paper to accumulate the resources available on state-of-the-art methodologies and is showcased for enthusiasts working in this domain.

The paper is organized in the following ways. Section II outlines the performance analysis of various FPGA prototypes processing the ECG signals available in the literature. Section III accumulates and diversifies the FPGA acceleration of ECG signals using CNN models, selectively reported on literature. Finally, concluding the discussion on state-of-the-art work reported on the topic for continuing further work, with a glimpse towards possible future activities in this direction.

II ECG signal performance analysis

This section is organized to discuss briefly the performance analysis of ECG signal high-lighting ECG signal compression, de-noising and various methods of classification in a few state-of-the-art FPGA platforms.

Association for the Advancement of Medical Instrumentation (AAMI) recommends five types of heart beats: normal beat (N), supraventricular ectopic beat (S), ventricular ectopic beat (V), fusion beat (F) and unclassified beat (Q) [7]. The different types of heart arrhythmias are Atrial Fibrillation (AF), Premature Atrial Contractions (PAC), Atrial Tachycardia, Atrial Flutter, Premature Ventricular Contractions (PVC), Ventricular Tachycardia (VT), and Ventricular Fibrillation (VF). The most common form of arrhythmia is premature ventricular contraction (PVC) [8] [9].

The fundamental stages of ECG signal analysis are, pre-processing, feature extraction and classification.

Pre-processing: In this stage ECG signal is made noise free to be further used for QRS complex detection. The various noises present in ECG signal are, baseline wander (electrode contact noise and electrode motion artifacts), power line interference (PLI), electromyogram (EMG) noise, and instrument associated noise. The filters used ECG signal filtration are: moving average, median, frequency-selective, adaptive, polynomial, and Wiener, and other methods like singular value decomposition (SVD), discrete cosine transform (DCT), discrete wavelet transform (DWT), empirical mode decomposition (EMD), nonlinear Bayesian filter, mathematical morphological operators, independent component analysis (ICA), nonlocal means method, variational mode decomposition and EMD-wavelet method [10]. The filtered signal is in the frequency range of 5Hz to 50Hz.

QRS complex detection: The detected QRS peak or complex is used for various feature extraction. QRS complex detection has been carried out in numerous ways available in literature; among them the most widely used methods Pan and Tompkin's algorithm (PAT), Wavelet transform, and sloping method for hardware implementation are highlighted here.

Pan and Tompkins algorithm (PAT) or modified version of it [11] [12] [13] [14], Sloping method-based techniques [15] [16] [17] [18] and Discrete/ Integer Wavelet transform based algorithms [19] [20] [21] [22] [23] [24] are verified on Xilinx System Generator for Digital signal processor (DSP) tool and implemented on various platforms of Field Programmable Gate Array (FPGA).

Feature extraction and classification: Extracted feature set and a variety of machine learning techniques like support vector machines (SVMs), naive Bayes, random forest, multiple layer perceptron (MLP), recurrent neural network (RNN) probabilistic neural networks (PNN), artificial neural networks (ANN) and deep neural network (DNN) have been used in literature to classify respected arrhythmias.

The QRS complex detection and feature extractions methods are implemented on various platforms of microcontroller [25] [26], Analog signal processor (ASP) is also found as an option for feature extraction in order to avoid intensive computation and more power consuming DSP-based techniques [27].

A tabular summary of the state-of-the-art techniques for analyzing various platforms has been reported in Table 1, citing available resources in literature. FPGAs have been chosen as an efficient option to validate various target applications, some of which are discussed in the following section.

1. ECG Compressor

An ECG compressor and decompressor is designed and verified on Terasic DE1-SOC platform embedded with ARM processor in Altera FPGA platform for MIT-BIH arrhythmia database in [28]. Here an 11 bit digitized ECG signal is generated at the output of an ADC and then prediction error is computed through the predictor. Two Huffman tables with six stages of look-up table are used to generate the encoded ECG signal, with a latency of 50ns. The maximum six ECG samples are compressed and packed into 16-bit words to be stored in a memory block. The total latency between capturing ECG signal and storing in memory is less than 14ms. The decompressor is implemented on ARM processor and correctness of the resulting signal is checked with original ECG signal.

TABLE 1 ECG PERFORMANCE ANALYSIS ON VARIOUS FPGA PLATFORMS

Paper	Database	Methodology/Model	FPGA Platform	Accuracy (in %)	Power	Target Application
[28]	MIT-BIH	Multi-Stage Huffman Coding	Terasic DE1-SOC	-	-	ECG compressor
[29]	InCarTDb	Pipelined Architecture with Probabilistic Neural Network (PNN) classifier	Zynq-7 ZC702	97	192mW (4classes)	Embedded ECG classifier
[30]	MIT-BIH	Artificial Neural Network (ANN)-Cardiac Arrhythmia Classifier (CAC)	Xilinx Pynq-Z2	98	13.34 µW	ASIC (0.18 µm CMOS) ANN-CAC classifier
[31]	Recording from Tongji Hospital (Huazhong University of Science and Technology, Wuhan, China)	Deep Convolutional Neural Network (DCNN)	Xilinx Zynq XC-7Z020	86.7	-	homecare ECG diagnosis

[32]	MIT-BIH	K-NN	Zybo Zynq 7000 (xc7z010clg400)	99.5	EigenDecomposition-1.857(100) SVD-1.725(100)	ECG based bio-metric system
[33]	MIT-BIH	Trace- STDP	Zynq-7020	83	230mW (4 classes of heart conditions)	Wearable Bio-signal Processor
[3]	Acquired ECG via ECG module AD8232	Modified PAT	Zynq-7000 Zybo	Real time observation	-	IoT enabled ECG monitoring system
[34]	MIT-BIH ECG Sensor VS100 and Shimmer3	AES & PCA	Xilinx ZC702	-	107mW	ECG based bio-metric system

2. ECG arrhythmia Classifier:

Probabilistic Neural Network (PNN) and Artificial Neural Network (ANN) based cardiac arrhythmia classifier (CAC) and the implementation on FPGA boards has been discussed here.

The authors in [29] have proposed a pipelined structure for embedded devices and smart systems with stages: de-noising, detection and segmentation of filtered ECG signal, dynamic morphological features extraction, and 5 types of heartbeat classification. The implementation utilized less than 30% of the FPGA resource usage.

The system is validated with InCarTDb database (from PhysioNet) featured with Lead 1 seventy-five 30-minutes recordings of 32 different patients data sampled at 257Hz, and a maximum 180 bpm heartbeat rate. In the design, the FIFO generates buffered ECG lead signal and digitized samples to batches of 500ms window size. Then another FIFO block stores the signal filtered through the Moving Average filter. Pre-processing is done for each sample batch with low-pass filter and normalization by comparing with peak amplitude value of the previous PQRS wave. Morphological Feature Extraction and Dynamic Feature Extraction Unit extract the features which are the input for Probabilistic Neural Network (PNN) classifier, resulting in the classified heartbeats: (i) normal beat (ii) APC (iii) RBBB and (iv) PVC.

This prototype is developed on Zynq-7 ZC702 Evaluation board with operating frequency of 35MHz, total power consumption found to be 192mW, 200mW and 208mW for 4, 8 and 16 classes of heart conditions with accuracy of 97%.

CAC-ANN designed in [30] introduced continuous-in-time-discrete-in-amplitude (CTDA) aiming to reduce number of multiplication, conditional grouping scheme (CGS) and biased training (BT) to manage the non-uniform imbalanced training samples of the MIT-BIH database, event driven approach to reduce input complexity, ReLU activation function, and arithmetic unit with only one multiplier based on 16-bit three-dimensional reduction multiplication (TDM) and 24-bit Sklansky-Tree (ST) adder for better power efficiency.

The Level-Crossing ADC (LC-ADC) does sampling based on event-driven approach and generates CTDA signal. Each generated sample is featured by two pulses and the time labels. The polarity of these pulses is presented with 1-bit (“1” or “0”) per sample, reducing the data volume to 91% as compared to 8-bit Nyquist ADC for CAC. This ANN-CAC has 3 layers ($32 \times 16 \times 5$) and takes 96 bits of input data frame, where two adjacent RR intervals are presented with 22 bits and pulses centered at R peak with last 74 bits. Training and verification is done in 7:3 ratio of the total samples of each record.

The ANN-CAC classifies N, S, V and F types by achieving 98% accuracy, 97% sensitivity, and 94% positive predictivity. The model is verified on Xilinx Pynq-Z2 FPGA board, with operating frequency of 2.5 MHz, and uses 5269 look up tables (LUT), 1024 LUT based RAM (LUTRAM) and 1311 flip-flops (FF). These resource usages are less than 10% of the total logic gate resources from Xilinx. The ASIC implementation of this design claims average power of 13.34μW for heart rate of 75 bpm, synthesized with 1.8V, 0.18μm CMOS process at 25MHz clock frequency. This implementation can work with frequency 10 KHz to 25MHz and resulting in lower leakage as the average current drops.

3. ECG monitoring system:

Targeting a real time ECG monitoring system, the prototypes implemented on FPGA board have been verified with acquired ECG signal. These have been performed using existing dataset as well as recorded signals from patient’s history.

Deep convolutional neural network (DCNN) based homecare directed ECG monitoring system is proposed in [31] with pruning scheme in channel-level a reduction of parameters up to the extent of 75.4% is gained. Parameters quantization helped to reduce

the floating-point operations by 42.7%. The design is implemented for 12-lead ECG raw signals classification on an embedded platform Xilinx Zynq XC-7Z020 FPGA chip, with two ARM Cortex-A9 processors and Artix-7 FPGA. For evaluation of the proposed DCNN model the dataset of 206468 ECG recordings from Tongji Hospital is distributed in random manner with 80%, 10%, and 10% for training, validation, and test sets, respectively.

The 3 main modules of proposed DCNN model are: 1) pre-convolution module 2) multiple-block CNN 3) multilevel classifier. This model is having convolutional layers of 13 stages and two subsequent fully connected (FC) layers. The first three convolution layers with kernel size 21, 32 filters and stride 2 are fed with long input data. The rest convolution layers stacked with kernel size 5, stride 1 and a filter size of 64 filters in the first group, and gradual increase up-to 256 by a multiplication factor 2. Fast down-sampling is done by three max-pooling operations in the last convolution block. Batch normalization (BN), and multilevel classification with ReLU activation function is done after each convolutional layer. Two dropout layers are added to the fully connected (FC) layers to address overfitting. At the end of the model, C-sigmoid activation functions are used to convert real values into class probabilities, and the binary cross-entropy loss function is applied.

The prototype of ECG detection system has ECG acquisition unit- ADS1298 and transmit raw signal sampled at 500Hz to STM32. Then the processed ECG recording undergoes noise elimination, normalization, quantization (8-bit integer), and then convolutional computation is done in the programmable logic (PL) part for of Xilinx Zynq XC-7Z020 FPGA chip.

The diagnosing time achieved for 10-s ECG data is 2.895s, F1 score is 0.913, the average area under the receiver operating characteristic curve (AUC), and the average specificity are 0.994 and 0.997 respectively, the average sensitivity 0.891, and exact match ratio, extension of the prediction accuracy 86.7%. This prototype being a wearable one has a major limitation with complex sensing component of 12-lead ECG sample collection system which can be improved with 3 or 6-laed arrangement.

In the work [3], an IoT based ECG monitoring system is proposed with optimized Pan and Tompkins algorithm, and implemented on Xilinx Zynq-7000 Zybo board. The patient's heart rate and temperature are measured by ECG module AD8232 and analog thermometer 3950 NTC (negative temperature coefficient) respectively. The heart rate and temperature computed are displayed in the web page with ESP8266 WiFi module using WiFi 802.11b/g/n operated at 2.4 GHz channel.

The collected ECG signal and temperature from patient's body are converted to digital signals through Xilinx Analog-to-Digital Converter (XADC) which is a dual 12-bit ADC. XADC is a part of the PL of Zynq device and it interfaces with PS through the PS-XADC interface. The IP core is created with modified Pan-Tomkins algorithm by eliminating the derivative and integration parts for QRS detection and heart rate measurement. The ECG simulator and the temperature sensor data received trough FPGA board are processed and displayed on the web page via the ESP module by serial UART-lite interface.

A wearable neuromorphic Bio-signal Processor is proposed [33]for four class arrhythmia detection using MIT-BIH ECG dataset. A single-layer excitatory inhibitory Spiking Neural Network (SNN) is modeled on unsupervised Spiking-Timing-Dependent-Plasticity (STDP) algorithm. The excitatory neurons (EN) receive spikes from input neurons through a fully connected layer, and then each EN connects to inhibitory neuron (IN) through positive weights in one-to-one connected layer. Each IN is connected with all EN except the previously connected one through negative weights. The input neuron is modeled with Leaky-Integrate-and-Fire (LIF) model and spikes have been generated based on the membrane potential. Based on the generated spikes, weights are updated and an event driven architecture is modeled.

The real time input and output events, reception or generation of input or output spikes are managed through Address Event Representation (AER) asynchronous protocol. The AER packets having spiking neuron ID and the respective timestamp are generated by AER bus and stored in two FIFOs. Three event handlers: Integrate Handler, Leaky Handler and File Handler are meant to work in event-trigger mode. To model low power architecture, the processor was only activated on completion of the previous event and set idle for rest cases.

The SNN model has 251 input neurons and 251 ENs, and time step of 100 to encode the raw ECG signal. The processor is implemented on Zynq 7020 FPGA platform and has achieved recognition accuracy of 83% on MIT BIH dataset. The processor has utilized 344 and 579, LUT and FF respectively, and the consumed power of 230mw.

Quite a few works available in literature has used CNN as an efficient metric for feature extraction of ECG signal, which has been reported for a brief understanding in the next section.

III FPGA AS ACCELERATORS FOR ECG SIGNAL CLASSIFICATION USING CNN

This section gives a short preview on various acceleration boosted by FPGAs for medical arena, specifically for the ECG signals classifying types of heartbeats. Table 2 shows the comparative list of articles depicting the summary of reported metrics. A brief zest of each article has been shown in the rest of this section.

For Real time ECG classification on low-powered edge devices Deep learning model- CNN is over-parameterized with huge volume of dataset and computational complexity. To get savings on computational effort, power usage and memory for storage, a group of recent works has introduced compression techniques like, sparse model, pruning scheme and binarized CNN for CNN implementation on FPGA.

The above-mentioned CNN models are implemented on both 1D and 2D. In literature 1D CNN models are less resource intensive compared to 2D CNN models, whereas 2D based models are robust to noise. The details of network arrangements are discussed in subsequent section.

In [35] the authors has used Pruning technology to develop a small-scale sparse 1-D CNN model with five significant modules: group of RAM, array of processing elements (PEs), pixel scatter, central controller and auxiliary circuits, and works on 16bit fixed point ECG data of MIT-BIH database.60% sparsity is achieved in input feature map by taking the non-zero indexed weight values. These weights, instructions, signal activations are transferred to on-chip RAM from external memory. The Pes takes one clock cycle for completion of one multiplication and addition. The non-zero weight and index distribution for respective PEs along with selection of data path is done by a weight decoder unit. The valid activation will be loaded to PE by MUX and shift register in Pixel (weight/ activation) scatter. The central controller generates the control signal for the pipelined operations of the PEs. The auxiliary circuits add bias; do the pooling, and truncating operations on the partial sum obtained from the specific data path.

This is implemented on Xilinx Zynq ZC706 FPGA platform, with an accuracy of 99.17% on five types of ECG beats (normal beat (NOR), LBBB, RBBB, PVC and APB) utilizing 1995 LUTs, 3011 FFs and 12 DSPs.

Three network pruning algorithms based on magnitude of weights and bias: a) simple pruning, b) fine-tuning based pruning c) multistage pruning with reference to a 3layered base-line CNN model are implemented in [36]. Zeroing and fine-tuning have been done on each layer of this model. They have evaluated performance and complexity with respect to different sparsity levels (η), ranging from 10% to 90%. They claimed of achieving accuracy of 98.12%, sensitivity of 98.07%, and specificity of 98.29% in classifying ECG into N, SVEB, VEB, F and Q standard through 10layers of the model. This evaluation may be extended for other datasets along with CNN models.

[37] This is paper aims to develop a flexible, efficient wearable ECG classifier based a small-scale unstructured 1D-CNN accelerator with 70% sparsity. It is designed with a tile-first dataflow excluding zero weight multiplications, for data compression and power gating on activation. A configurable array of four 12-stage cascade, 32-bit instruction processing element (PE) is designed for multiplication of weights and addition of bias of a tile. This model supports pipelined processing of multiple pooling types (none, max pooling, average pooling and global average pooling (GAP)), varying kernel sizes and number of feature maps. The accelerator can be a good option for wearable ECG device with computing efficiency of 118.75% and energy efficiency of 3.93μJ per classification by completing a beat classification in 4.6ms under 2MHz clock frequency.

A wearable Artificial Intelligence-of-Things (AIoT) device targeting to classify ECG excluding feature extraction or pre-processing steps is modeled in [38]. 2D-bCNN classifier for classifying class 1 for the true label all related V beat and the rest as class 0 is modeled with quantized multi-layer perceptron (qMLP) and bCNN perform image generation and image classification, respectively. The model categorized as better performance (BP) and low power (LP) models taking the image of size 16×20 and 10×10. The dense network qMLP consists of 3 layers. The first layer, qDense1 takes 11-bit ADC output and multiplies with quantized 8bit weights and accumulates. The activation unit quantized rectified linear unit (qReLU), quantized the 32-bit accumulator output to 8bit. qDense2 layer performs the multiplication and activation using qRelu. The output of qDense3 layer uses binary hyperbolic tangent (bTanH) and generates binary inputs for the succeeding bCNN layer to perform multiplication operation with XNOR logic and deployed sigmoid activation function to find generation loss (GL). The bCNN classifier finds the classification loss (CL) and classifies the binary image as V or non-V beat deploying bCONP (convolution and pooling), bDense1 and bDense2 layer with sigmoid activation function. The device chosen for implementing model is Lattice Semiconductor's ultra-low power iCE40 UltraPlus iCE40UP5k. The accuracy is 98.5% and 98.2%; sensitivity is 85.4% and 80.6%; and F1 score is 89.2% and 86.2% for BP and LP model respectively. Dynamic power consumption by BP and LP models are of 55.4 μW and 34.9 μW; and static power are 377.9 μW and 376.6 μW, respectively at 100 kHz. This proposed CNN model comparatively uses less MAC operations and made it preferable for wearable edge IoT device.

Resource constrained FPGA may be an attractive option for accelerating CNN models for ECG classification with scaling down the input feature map or the introducing quantization in various layers.

IV Conclusion

The state-of-the-art technologies used for classifying ECG signal using FPGAs as accelerators previews the power of resource constrained devices that can be utilized in the health sector domain. Taking advantage of convolutional neural networks, various applications can be tapped and a huge market can be explored. This paper gives a glimpse of ongoing activities in this domain of CNN based classifications with the assistance of FPGAs as accelerators to diagnose small variations of ECG signals. Further activities to understand heart beats in a large scale can be done in the Internet of Things arena, where sensors and actuators can securely communicate with the server cloud without hampering the data.

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