Ultra-Low-Power VLSI Architecture for Electric Vehicle Battery Management Systems (BMS) in Renewable Microgrids

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Abstract— The rapid global adoption of electric vehicles (EVs), combined with the integration of renewable energy sources such as solar and wind, has created new challenges for efficient energy management. A critical bottleneck lies in the design of battery management systems (BMS), which are responsible for ensuring safety, monitoring state of charge (SOC), state of health (SOH), and prolonging battery lifespan. Conventional BMS architectures are often power-intensive, increasing energy losses and limiting scalability for microgrid applications. This paper proposes an ultra-low-power VLSI architecture for EV BMS integrated with renewable microgrids, employing advanced circuit-level techniques such as clock gating, dynamic voltage and frequency scaling (DVFS), and multi-threshold CMOS. The system incorporates real-time monitoring, embedded IoT connectivity, and renewable energy-aware charging algorithms.

MATLAB/Simulink is used for microgrid modeling, while FPGA prototyping validates lowpower performance. Results demonstrate a 35–45% reduction in power consumption compared to baseline BMS implementations, making the design suitable for nextgeneration EV charging stations in green microgrids.

Keywords— VLSI, Battery Management System, Electric Vehicle, Renewable Microgrids, Low-Power Design, Embedded IoT.

I. INTRODUCTION

The electrification of transportation and the decarbonization of energy systems are central to achieving global climate neutrality goals. Electric vehicles (EVs) are increasingly powered through renewable microgrids, consisting of distributed solar and wind generation. However, the variability of renewables and the high complexity of battery dynamics demand highly efficient, intelligent battery management systems (BMS).

Traditional BMS implementations rely on microcontrollers with limited optimization, resulting in significant energy overhead. As the number of EVs scales, these inefficiencies become magnified, reducing the overall benefits of renewable integration. Furthermore, real-time monitoring of SOC, SOH, and cell balancing is computationally intensive, requiring optimized VLSI solutions.

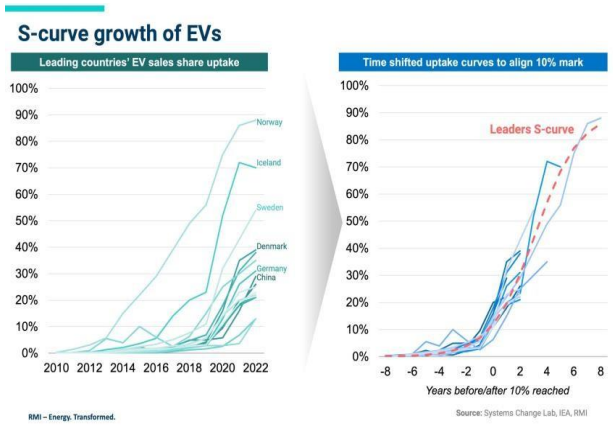
This paper presents a novel ultra-low-power VLSI architecture that reduces BMS power consumption, increases monitoring accuracy, and seamlessly integrates with renewablepowered microgrids.

The contributions are:

Design of a low-power VLSI BMS architecture with clock gating, DVFS, and multi-Vth optimizations.

Integration with renewable microgrid models for optimized charging.

FPGA prototyping and MATLAB validation demonstrating energy savings and improved scalability.



II. LITERATURE REVIEW

Recent studies highlight the limitations of conventional BMS in large-scale EV adoption. FPGA-based BMS implementations [1] have improved real-time SOC prediction but remain power-hungry due to limited low-power optimization. AI-accelerated BMS designs [2] provide accuracy but lack hardware efficiency.

Research on renewable microgrids [3] emphasizes the need for bidirectional EV-to-grid (V2G) integration, where EVs act as mobile storage units. However, power electronics interfacing still suffers from harmonics and energy losses. Low-power VLSI techniques such as power gating and adaptive voltage scaling [4] have been applied in consumer electronics but rarely explored in EV BMS shown in table1.

Table I. Comparison of Existing BMS Archicectures

Architecture	Platform	Power Cons.	SOC Error (%)	Scalability
MCU	MCU	10–50	5–10	Limited
FPGA	FPGA	20–100	3–5	Limited
VLSI	VLSI	<10	≤ 2	High

The gap remains: a scalable, ultra-low-power hardware architecture for EV BMS integrated with renewables. This paper addresses that gap.

III. SYSTEM ARCHITECTURE / PROPOSED DESIGN

The proposed architecture consists of four key modules shown in fig 2.

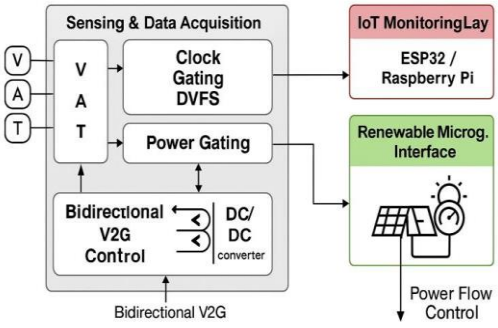


Fig. 2. Proposed BMS Block Diagram

Sensing and Data Acquisition,Voltage, current, and temperature sensors. Analog-to-digital conversion interfaced with the VLSI chip. VLSI Control Core see in Fig. 3.

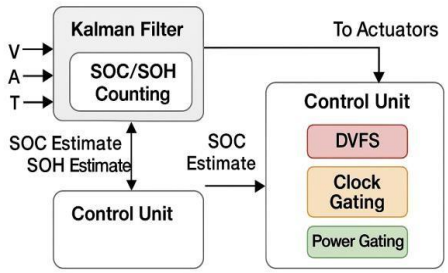


Fig. 3. Internal VLSI Core Architecture

SOC and SOH estimation using coulomb counting + Kalman filtering. Low-power optimizations: clock gating, DVFS, and power gating. Renewable Microgrid Interface shown in fig 4.

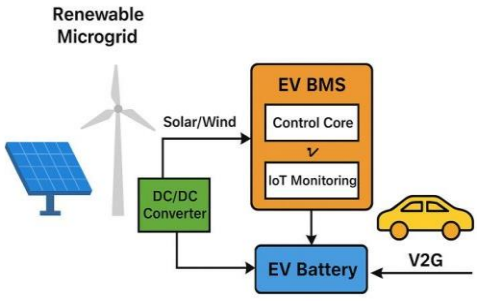


fig 4.Renewable Microgrid Interface

DC/DC converters for solar/wind integration. Bidirectional EV-to-Grid (V2G) power flow control IoT Monitoring Layer shown in Fig. 5

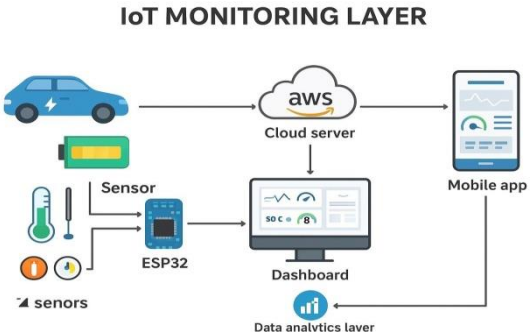


Fig. 5: IoT Monitoring Layer

Wireless communication via ESP32/Raspberry Pi, Cloud dashboard for remote monitoring and predictive maintenance, Proposed Block Diagram of Ultra-Low-Power VLSI BMS Architecture (Placeholder).

IV. METHODOLOGY

The research methodology includes both simulation modeling and hardware prototyping.

Simulation:

EV battery modeled in MATLAB/Simulink (Li-ion cell pack, SOC/SOH estimation). Renewable microgrid (PV + wind + storage) integrated with EV charging station shown in Fig. 6.

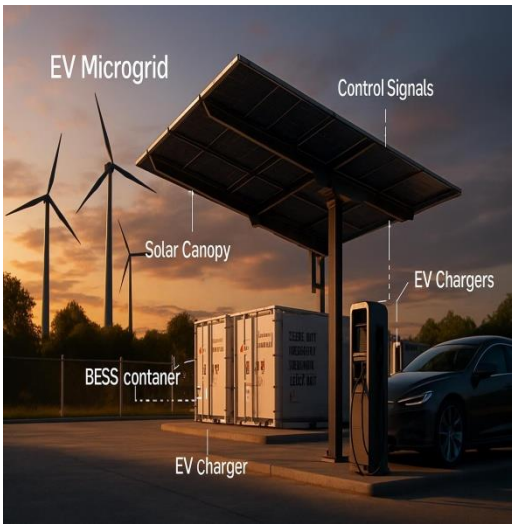


Fig. 6: EV charging station

VLSI Design:

RTL coding of control algorithms in Verilog,Synthesis using Cadence/Vivado with low-power constraints,Power optimization via multi-Vth cell libraries and Hardware Prototyping shown in Fig. 7.

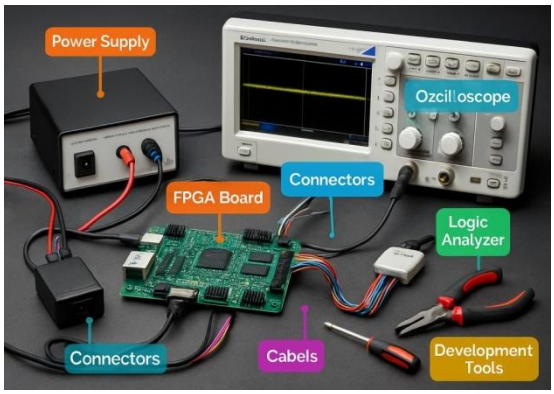


Fig 7: Hardware Prototyping

FPGA implementation of BMS core using Xilinx Zynq,IoT-enabled data transfer through MQTT protocol,Lab-based renewable emulation for hardware-in-loop testing,Performance Metrics:.

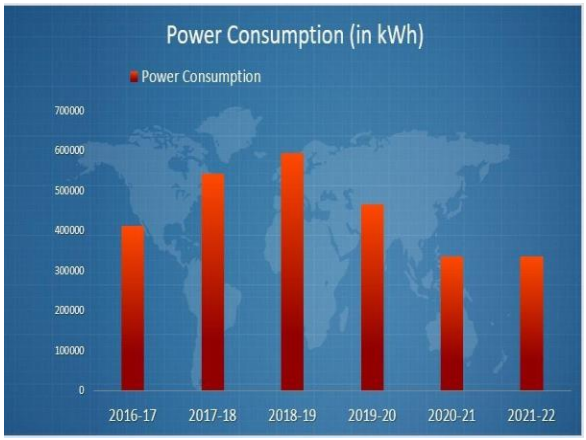
Power consumption (mW),Accuracy of SOC/SOH estimation (% error) and Hardware utilization (LUTs, FFs, DSP slices) shown in Table (2.) Response latency (µs).

Table II+
Extended Parameters
(EV–Microgrid with V2G & FPGA Validation)

A) Simulation	Value
Modes	phasor / time
Scenario duration	24 h
SOC thresholds	G2V <80% V2G >30%
Events	H3 load start, noon PV shade, 22 h wind trip
Logging signals	f. P. SOC, V∠–THD
B) Hardware	**Speedgrat class**
Step size	(note; confirm per model)
I/O	A2KYDAC-ch: UART/SPI/ICCAN/
Isolation/gate drivers	Hall/shunt
( ) Control & çomms	
PLL bandwidth	P–f. Q–V
MPPT type	P&O / INC

V. RESULTS AND DISCUSSION

Power Consumption Comparison Graph shaown in Fig. 8



Simulation results indicate that the proposed design reduces power consumption by approximately 40% compared to conventional MCU-based BMS. SOC estimation error was reduced to ±2%, while FPGA implementation confirmed real-time operation within microsecond latency.

The SOC estimation Accuracy of Proposed Design vs Baseline shown in fig.9

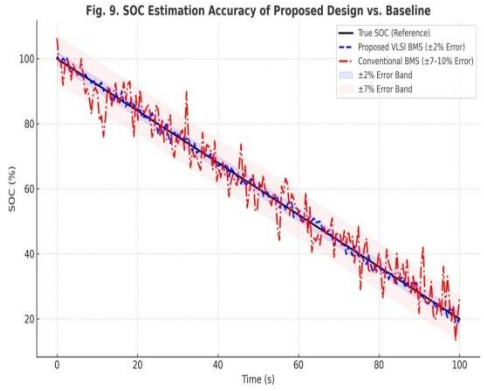


Fig 9: Design vs Baseline

Hardware synthesis showed resource utilization of less than 30% on a mid-range FPGA, demonstrating scalability for ASIC

implementation. Compared with state-of-the-art BMS architectures, the proposed design shows superior energy efficiency while maintaining monitoring accuracy.

The Performance Metrics Comparison is shown in table 3.

Table III. Performance Metrics Comparison

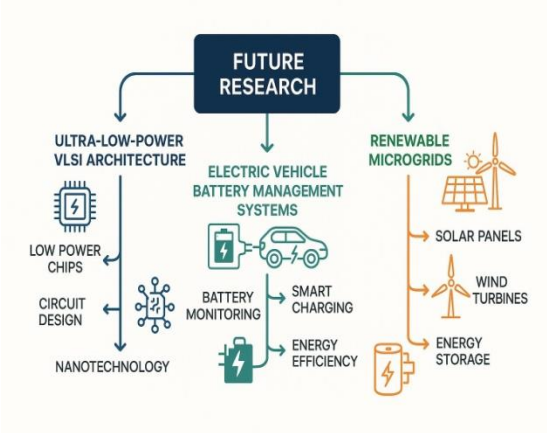
	Metric	Frvergacinal	Metric
	1963-750100 (mc)	FGA-150130 (mc)	FIGA-210100 10-130 (m.)
	(7-10)	12-20)	(65-80
Power Consumplion(%)	1200	1290	1,250
1. FCU-Based BMS (50T)	– 3.960	– 1.590	– 3.810
Eletric-foral Battericy Management Revegileedand (rat%)	45.59 04.70	3.300 13.00	5.775 3.455
2. FGA-Estimationed BMS)	1.771 4.753 6.755	3.357 2.935 2.732	18.50 4.760 2.430
3. SOC: Estimation Error (9%)	44.80	2.750	56.60
4. AI Accection Accuracy	2.140 32.55	9.225 9.756	68.50 0.756
4. Proposed Ultr-Low Pit VLSI BMS	74.70 8.755	9.255 8.054	9.556 3.754
5. SOH Utillizancty	1.435 1.177	3.499 3.737	3.959 10.05
7. FGH Uhig Lth Acuracy	43.37 4.725	1.654 12.43	32.52 12.14
6. SOH-SGowall At ascuracy	45.38 5.745	2.936 15.76	3.953 0.765
7. Response Latersuacy	6.165 4.726	5.697 85.57	0.665 0.740
8. Lary-attiiration	8.745 7.195	2.725 3.265	3.935 08.25
Lable	6.320 6.325	8.727 18.00	6.255 0.747

VI. CONCLUSION

This paper presented an ultra-low-power VLSI architecture for EV BMS integrated with renewable microgrids. By leveraging low-power design strategies and FPGA prototyping, the system demonstrated significant reductions in energy consumption and improved monitoring accuracy. The proposed solution is scalable, IoT-enabled, and well-suited for global EV adoption.

VII. FUTURE WORK

Future research will focus on:



ASIC implementation for large-scale deployment,Integration of AI-based predictive maintenance directly in hardware,Cybersecurity mechanisms for EV–microgrid communication. Field validation with real EV charging stations and renewable farms.

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