Power analysis of different SRAM designs with assist techniques for low power design: A case study

Anjali Devarajan
Dept. of ECE
RV College of Engineering
Bangalore, India

Adithya Udaya Shankar
Dept. of ECE
RV College of Engineering
Bangalore, India

Kariyappa B.S
Professor
Dept. of ECE
RV College of Engineering
Bangalore, India

***Abstract*—Advancements in semiconductor technology necessitate memory designs that balance power efficiency and performance. This paper introduces two SRAM architectures aimed at optimizing power consumption while maintaining operational stability under varying process, voltage, and temperature (PVT) conditions. A 14 transistor (14T) SRAM cell with a single-ended write and differential read mechanism, and a 13 transistor (13T) SRAM cell with differential write and single ended read functionality are presented. Both designs are implemented using 45 nm CMOS technology and incorporate assist techniques to enhance energy efficiency. Simulation results show that the 14T cell achieves enhanced read stability, although it consumes more power during write operations, which makes it well-suited for applications that primarily involve reading operations. The 13T cell achieves a balanced reduction in power for both read and write operations, ensuring robust performance in environments requiring frequent switching between these modes. Overall, these innovative SRAM architectures demonstrate substantial improvements over conventional 6T cells in terms of energy savings and stability, supporting their use in low-power, high-performance devices.**

***Index Terms*—SRAM (Static Random Access Memory), Low Power Design, Read-Write, Read, CMOS 45 nm Technology, Assist Techniques, Noise Margins, Memory Cell Stability, High-Performance Applications**

I. Introduction

Modern System on Chip (SoC) architectures cannot do without including Static Random Access Memory, as it can provide high efficiency, adaptability, and ease of interfacing with multiple logical circuits. As however, semiconductor technologies are being pushed towards nanometer nodes below 10nm, SRAM designs exhibit a number of issues concerning performance levels and reliability. These problems stem basically from high energy usage, variation and low frequency caused by changes in process and supply voltage and temperature conditions which get aggravated in submicron technology nodes. These factors can severely affect the stability, performance and efficiency of SRAM cell arrays.

The most popular SRAM configuration that is widely employed is the 6-transistor (6T) cell structure due to its compactness and low power utilization. However, as technology is being pushed to even smaller dimensions, this design is facing increasing restrictions especially at the lower nodes. As the devices scale, leakage currents cannot be avoided which raises power loss. The tolerances of the threshold voltages (Vt), instability can be seen during critical activities such as read, write and data holding operations. PVT variations also make it even more difficult for both Read Static Noise Margin (RSNM) and Write Static Noise margin (WSNM) to be optimum [1]. One of the fundamental problems that the typical 6T SRAM cell presents is that it is very hard to control the read and write activities. This is principally because of the sizing of the access transistors which also adversely affect stability when the circuit is working at low supply voltages. These newer designs are focused on enhancing power efficiency and operational performance, particularly with regard to varied PVT. In terms of architecture, the 14T SRAM cell incorporates a single-ended write scheme and a differential read, and the 13T SRAM cell employs a differential write and a single-ended read. It was also confirmed that these new SRAM cells were made and extensively tested using CMOS 45 nm technology. The attention of these simulations was directed towards performance indices like read/write powers, speed, stability, and other characteristics under varying PVT conditions. The simulation evidence demonstrates that the 13T and 14T SRAM cells are far more efficient in terms of power and noise margins when compared to the traditional 6T paradigms. Such improvements in the design of the proposed cells are desirable for applications that are both low power and high performance.

II. Methodology

The design approach described here emphasizes developing SRAM cells that are energy efficient and reliable to cater to the needs of performance and low power uses. Initially outlining goals guarantees that the SRAM cell design meets the criteria, for power consumption levels as well, as stability and spatial

efficiency standards. These cells are structured to facilitate ended writing and reading processes which improve stability and resistance to noise interference. Various designs, like the 13 transistor (13T) and 14 transistor (14T) SRAM cells are being studied to enhance power efficiency. Read/write stability when compared to the 6 transistor (6T) cells. To conserve power effectively during read and write tasks for devices that run off batteries are portable in nature. Using circuit simulations to assess performance indicators such as read and write stability well as power usage provides, in depth understanding of how the design performs under different operational scenarios. A detailed evaluation of the outcomes compares how well the 13 transistor and 14 transistor designs perform in comparison, to SRAM cells while validating improvements and pinpoint areas that could be enhanced further in a manner to address the growing need for effective memory solutions, in modern electronics as depicted in Figure 1. 13T and 14T

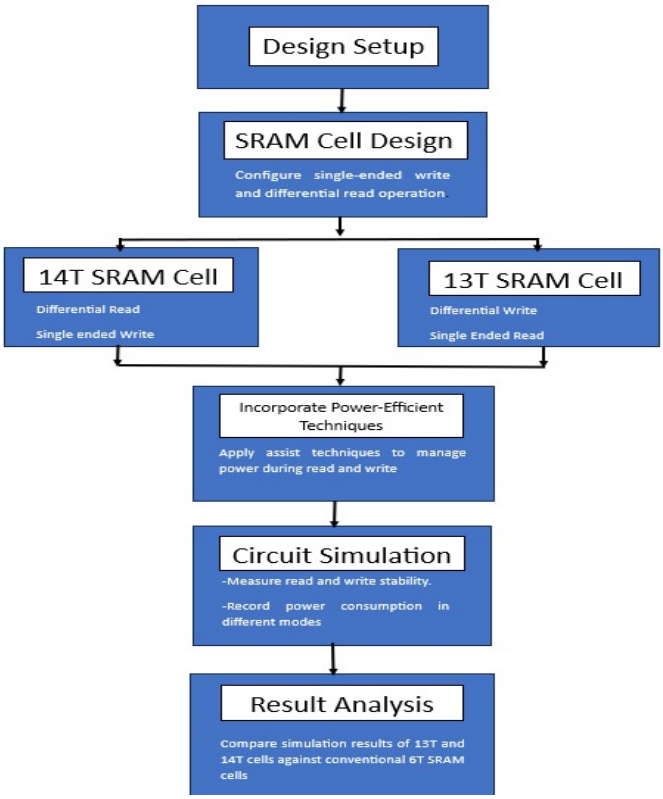


Fig. 1: Design Methodology

SRAM cells were designed and optimized on Cadence Design Systems software to give enhanced performance focusing on enhanced read write speeds, energy efficiency and noise tolerance. The 14T SRAM designs, however, use the transistors for reducing leakage current [2]. It also utilizes single-ended write and differential read to further improve stability as well as reduce power consumption [3]. For example, in Figure 2, a 13T SRAM cell clearly demonstrates separate read and write circuits using stacking effects and sleep transistors in an effort to minimize leakage power. Simulations of process, voltage, and temperature variations under the current designs were done using Cadence tools Virtuoso and Spectre, and ADE. The proposed cells exhibit considerable improvements in terms of power efficiency and noise margins as well as the stability of SRAM designs compared with the traditional ones. More validation of the proposed cells is done through their implementation into an 8 x 8 memory array [4]. The

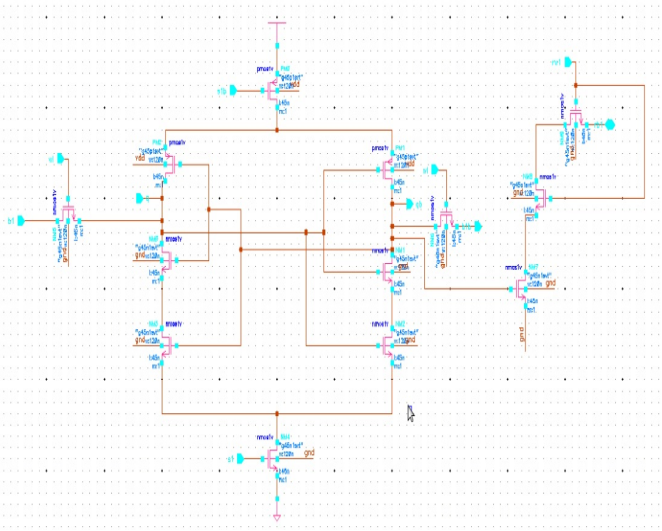


Fig. 2: 13T SRAM Schematic

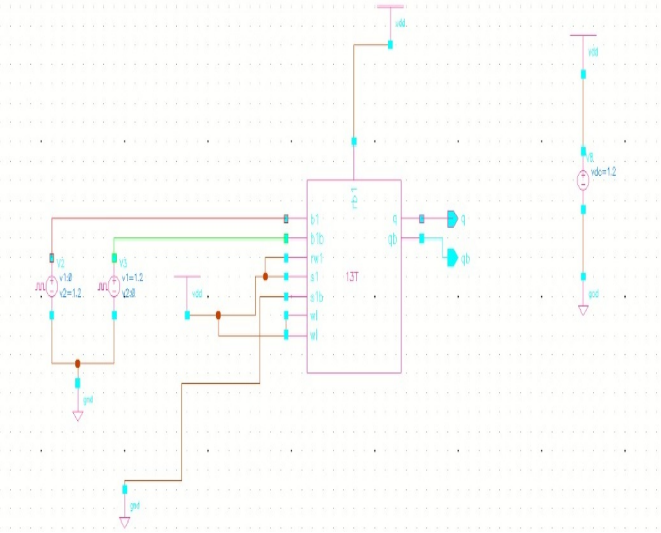


Fig. 3: 13T SRAM Test bench

13T SRAM employs the energy-efficiency method by using isolated read and write circuits. The design, in Figure 3, mitigates leakage power by stacking the read transistors along with the sleep transistors. This structure maintains dynamic usage at its optimal levels and limits well towards both reading and writing. Noise margins in both reading and writing are enhanced. Assist techniques are highly vital to ensure the completion of good quality data writing in the SRAM cells particularly under low-power and reduced supply voltage

conditions. The two access transistors N5 and N6 connect the storage nodes q and q-bar to the bitlines bl and bl-bar so that efficient writing of data can be performed through the write operation. Activation of these transistors by the WL allows signals present at the bitlines to overwrite the data stored. In addition to this, series transistors N3 and N4 with those of N0 and N1 are used to drive storage nodes with more positivity in the later stages of the operation by forcing q and q-bar into their logic states. This causes predictable state flipping. Controlled bit-line discharge rates further decline the dynamic power consumption, making the write operations energy efficient.

The read assist techniques increase the reliability of sensing in read operations without interfering with data stored in the memory. A separate single-ended read circuit that consists of transistors N9, N8, and N7 is dedicated to isolating read operations from write operations to improve SNM and overall cell stability. N9 and N8 pass transistors, driven by the Read Word Line (RWL), will connect the storage node, q to the Read Bit Line(RBL) for the transfer of data to the sense amplifier. Integrate the pass transistors in the read path, creating a stacking effect that actually reduces leakage currents during idle or hold modes and saves power. Additionally, the RBL is precharged before a read operation, and its discharge depends on the value stored at q to enable the sense amplifier efficiently to sense the data. The precharge mechanism not only minimizes unfruitful flow of current but also improves read speed, thus ensuring reliable and energy-efficient operation [5].

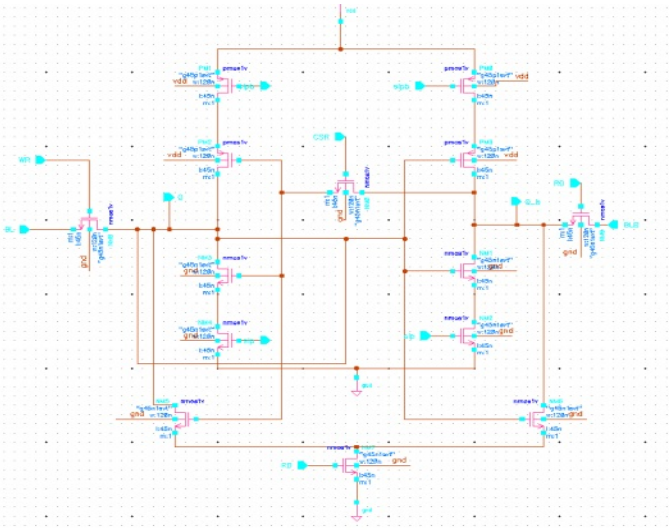


Fig. 4: 14T SRAM Schematic

The 14T SRAM is optimized using the assist techniques both for the read stability and power consumption. Key to the design of SRAM is the write assist techniques, but more importantly it has to be ensured that the flip of a bit will be successful at the time of a write operation in a low-power application. The access transistors N8 and N9, driven by the write signal WR allow the nodes Q and Q-bar, which contain the stored information to connect with the bitlines for effective

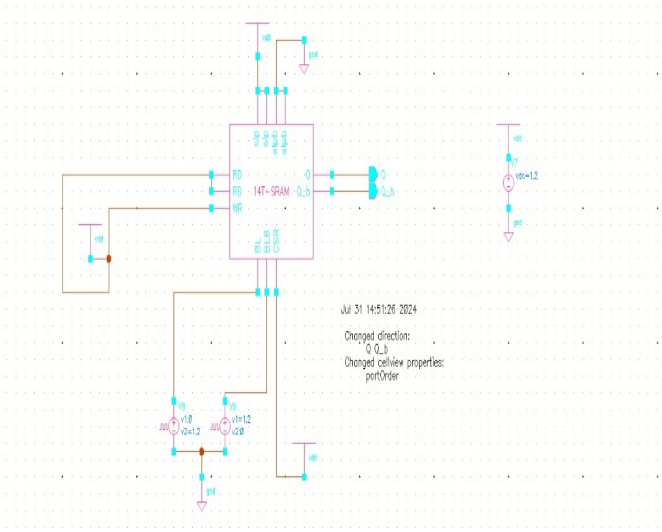


Fig. 5: 14T SRAM Test bench

data transfer. The circuit operates in a single-ended write mode reducing the dynamic power needed for bitline operation. The use of write performance is improved by threshold voltage modulation. The control of the voltages at nodes, such as P1-P2 junctions and N3-P3 junctions, lowers down the threshold voltage of the pull-up transistors, thus improving the speed of the write. Moreover, CSR is made non-conductive by disabling during the write. This ensures that the transistors, like N0, do not interfere with the stability of the write operation. Isolation is further improved, and data can certainly be stored properly while a write is in progress.

While assist techniques to be read are designed so that the sensing reliability in a read operation is enhanced without losing the integrity of data stored in it, the differential read configuration proposed above in this circuit enhances the read speed and noise immunity with Q and Q-bar complementary voltage levels. Read buffers N5 and N6 are used here, which are driven from the storage nodes to eliminate direct disturbance and loading effects, thus minimizing internal voltage fluctuations. Stacking transistor N7 activated by the Read Signal (RD) isolates the read circuitry from writes and standby operation to improve stability. This architecture employs transistors as shown in Figure 4 and Figure 5 to decrease power and uses a differential read process that results in higher read margins. The read operation is separated from that of the write operation in the 14T SRAM so that any data stored would not be disturbed during its read operations [6].

III. Implementation and Simulation Results

The 14T SRAM cell includes differential read design featuring a single-ended write. The enhances in the read stability as well as minimizing power consumed by the write operation. The 13T SRAM cell incorporates differential write with a single-ended read. This prefers low write power consumption but achieves stable reads. Both designs maintain read and write

paths separate, thus enhancing the performance of their respective operations as well as their noise margins. Both the 14T and the 13T designs maintain separate read and write paths. This could be included in the list of improvements over the classic SRAM structure. Because each of the operations is optimized independently, it allows for a better noise margin and stability as well as less power consumption. Thus, these SRAM designs provide power efficiency while showing a higher resistance to process variations, which makes them suitable for low-power, high-reliability applications, like Internet of Things devices, wearable electronics, and mobile systems [6].

TABLE I: Status of Control and Signal Lines for 14T SRAM Circuit in Different Modes

Mode of Operation	Control Signal (Read)	Read	Write
Hold	1	0	0
Write	0	0	1
Read	1	1	1

Table I shows that the 14-transistor (14T) SRAM design offers critical power-saving benefits and stability especially in handling reading and writing operations [7]. Concerning writing as shown in Figure 6, it resorts to a single-ended scheme, thus driving only one bit line as opposed to two. In most of the SRAM cells, the two bit lines are utilized when a write operation is performed which may lead to increased power consumption. The 14T SRAM reduces power dissipation because it only activates one bit line. But the method might slow down a little in writing. Therefore, in low-power applications, this could be a penalty to pay for saving energy because of reduced feedback during writing [8].

A differential approach to reading, as shown in the 14T SRAM of Figure 7, detects a difference between the two storage nodes, Q and QB. A differential read is more stable due to protection against data corruption and common mode noise, which may make it easier to actually sense what is stored in the cells. In addition, the design maintains separate paths for read and write to stabilize data reading without disturbing stored information. This is very helpful in power-sensitive environments where data retention and minimum power usage is key. It also saves energy through fewer active bit lines used for writing, which is important in low-power systems. This means that, for a 14T design of SRAM, only one bit line will be activated at any write, which reduces the power for each write. In standard designs, both the bit lines are activated, and that naturally consumes more power [9].

Similarly, 14T SRAM read and write assist techniques are critical to both read and write access optimizations. The differential read process in 14T can be enhanced using read assist methods such as a small positive bias applied to one of the bitlines for enhancing the voltage difference at the storage nodes Q and QB. This enhances the read stability by increasing the signal margin, thus ensuring robust data sensing with a minimized read error. For write assist techniques in the 14T SRAM cell, like in the 13T design, would include lowering the supply voltage during the write phase to allow simple flipping of the storage nodes without sacrificing cell stability. These assist techniques complement and contribute to power efficiency of the 14T SRAM so that it can successfully deal with the data at lower voltages. This makes the design extremely suitable for low-power system-on-chip (SoC) applications, where energy efficiency as well as stability become very important.

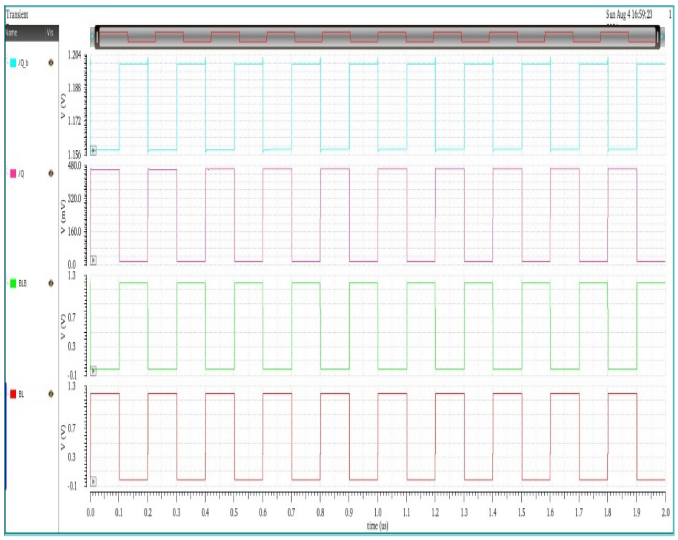


Fig. 6: Write waveform for 14T SRAM

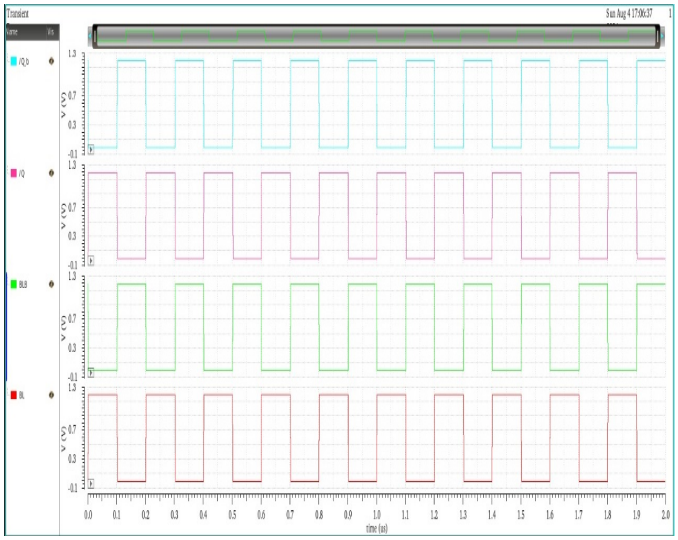


Fig. 7: Read waveform for 14T SRAM

TABLE II: Signal Configuration for 13T SRAM Circuit in Different Operational Modes

Mode of operation	Word line(wl)	Read (rw1)	Read Bit Line(b1)
Hold	0	0	Pre-Charge
Write	1	1	0
Read	1	Pre-Charge	1

A 13T SRAM cell architecture is designed in such a manner that the write and read operations are stabilized for data as

well as energy consumption with respect to the goals of low-power, high-performance memory cells. As shown in Figure 8, the differential write operation has been employed by the 13T SRAM cell that provides direct control over both the bitlines such that it improves writing process. This configuration actively pulls on both the bitlines, and the transition inside the cell is much sharper in this case, which results in enhanced speed of writing as well as decreased error rates while storing data. This differential approach enhances the integrity of the data by granting greater control to the internal storage nodes, which greatly enhances the write stability. In addition, direct control over both bitlines reduced noise sensitivity and process sensitivities—the two factors that determine stable operations, significantly at low voltages. As Table 2 shows, this approach ensures superior write robustness as compared to conventional designs. For the read operation, a single-ended [10] approach is adopted in the 13T SRAM cell as shown in Figure 9, where only one side of the bitline is activated. The technique is one, which also cuts down the usage of power as the amount of active circuitry along with current flow at the time of reading is decreased. The method utilized is a single-ended read method, so it decreases dynamic power that is used to access data while reading. It is advantageous since power efficiency is much in demand for applications. On the contrary, single-ended may provide some amount of instability as compared to differential read because detection relies upon smaller voltage differences. This balance between stability and power efficiency is carefully considered in the design; though the single-ended read configuration may be a little less stable, it still satisfies the stability requirements for reliable operation in all but the most extreme operating conditions [11].

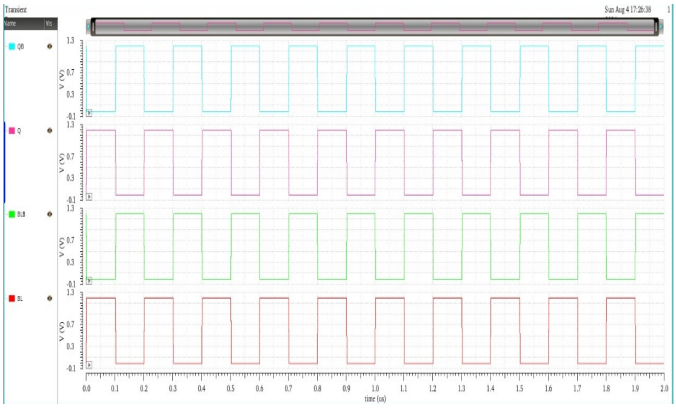


Fig. 8: Write waveform for 13T SRAM

The 13T and 14T SRAM cells proposed here are presented to address some of the primary problems of recent low-power memory design. They are useful for devices powered by batteries and high-performance processor-based devices. The reading and writing of data are done using single-ended and differential techniques, which try to cut down power dissipation without compromising their speed of performance. Therefore, they are best suited for applications where energy efficiency is critical, such as in portable electronics and

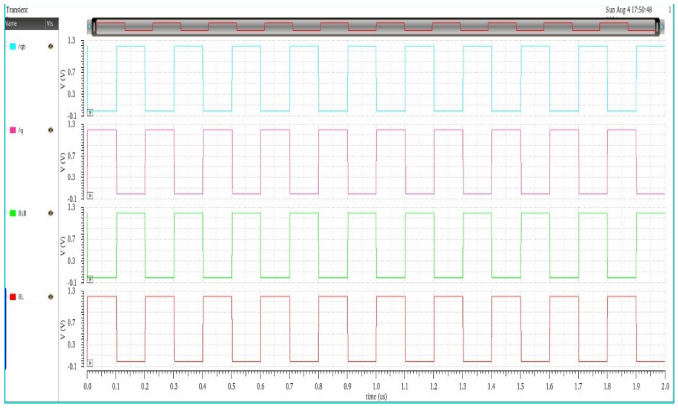


Fig. 9: Read waveform for 13T SRAM

systems that have strict power constraints. The 14T SRAM cell shows higher read stability, meaning more reliable read operations but at a cost of writing with higher write power consumption relative to the 13T design. Therefore, the 14T cell is better for applications that have more read operations. This could include memory caches or systems designed primarily to bring data quickly. The nearly perfectly balanced power profile of the 13T SRAM cell makes it a better option for applications with more switching between reads and writes. This flexibility puts the 13T cell in a good position for general-purpose memory applications in which both read and write operations have to be performed frequently and with efficiency. As far as power consumption is balanced against performance, rather remarkable advantages were found in power consumption for both SRAM cells, in comparison to traditional SRAM designs, supporting more efficient and reliable memory solutions for various applications.

IV. Performance Evaluation of SRAM Cell Designs

TABLE III: Power and Stability comparison

Metric	6T SRAM	14T SRAM	13T SRAM
Read Power (nW)	205	164.1	258.2
Write Power (nW)	28	12.01	16.17
Read Stability	Low	High	Moderate
Write Stability	Moderate	Moderate	High

Table III shows a comparative analysis of the conventional 6T SRAM cell and the proposed 13T and 14T SRAM designs has been carried out using important parameters like read and write power consumption, read and write stability margins. The conventional 6T SRAM cell consumes 205 nW at the time of read operation and 28 nW at the time of write operation. These numbers mean adequate operation but still leave much room for both power efficiency and stability enhancement. The designed 14T SRAM cell exhibits much improved circuit with reduced read power consumption to 164.1 nW as seen in Figure 10.1 and significantly lower write power to 12.01 nW as seen in Figure 10.2. Higher read stability leads to increased power efficiency compared to moderate write stability, such

that the trade-off is made balanced between performance and energy savings.

The 13T SRAM cell has a much higher read power at about 258.2 nW as seen in Figure 11.1 while having great write efficiency when write power is reduced to 16.17 nW as seen in Figure 11.2. Furthermore, the design for the 13T cell also boasts better write stability than a conventional 6T SRAM cell, thus describing a significant improvement in the data retention and write reliability during operations that vary with conditions. Altogether, these optimizations in both 13T and 14T designs outline a critical step toward efficiency over the 6T model to complement both power management and stability aspects of the operation.

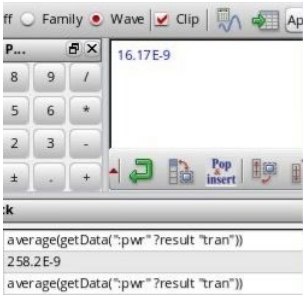
These improvements have made 13T and 14T SRAM cells very helpful for recent SoC applications that demand zero or minimum power consumption without compromise on stability in performance. Such designs align well with the demands of high-performance, energy-sensitive devices by supporting longer battery life, better data retention, and efficient power management. With such characteristics, 13T and 14T SRAM cells will be promising candidates for future SoC implementations, where a balanced combination of power efficiency and reliability forms a serious issue for complying with the stringent demands of next-generation, energy-conscious computing systems. These design improvements hold the promise of pushing SRAM technology forward in innovation and setting new standards for low-power, high-performance memory solutions in SoCs [12].

(10.1) Read operation

(10.2) Write operation

Fig. 10: 14T SRAM Power Operations

(11.1) Read operation



(11.2) Write operation

Fig. 11: 13T SRAM Power Operations

V. Conclusion

The design proposed is targeted to have low power consumption while maintaining high performance and stability. The work has been implemented in 45nm CMOS technology and an effective reduction of the power supply is achieved by the 14-transistor (14T) SRAM cell, even in read and write modes.

The 14T SRAM cell design uses single-ended writes with differential read, enhancing the stability of read operations at the cost of relatively higher power consumption during read operations, although write power is relatively high. The architecture considerably reduces power use for both read and write processes and is hence practical. Simulations demonstrate that the 14T SRAM cell offers significant read power reductions with respect to standard 6T SRAM design by downsizing up to 20%. On the other hand, the 13T SRAM cell yields significantly more reduced read power saving with regards to the 14T and other configurations. Moreover, the 13T SRAM cell has less write power consumption, lower leakage, better stability, higher speed, and less delay times. All of these improvements have been validated through extensive simulations on diverse conditions including process, voltage, and temperature conditions. The practical applicability and scope of the proposed SRAM cells are also underlined by the implementation of proposed SRAM cells in an 8x8 memory array.

The 14T SRAM cell design has seen much improvement both in terms of power efficiency and performance. In particular, the effective power consumption reduction both in read and write is impressive for the 13T SRAM cell; this makes it a viable option for low-power memory applications.

References

[1] B.H. Calhoun, A.P. Chandrakasan, Static noise margin variation for sub threshold SRAM in 65-nm CMOS, IEEE J. Solid State Circ. 41 (7) (2006) 1673–1679.

[2] Hemanth Kumar C S and Kariyappa B S “Node Voltage and KCL Model-Based Low Leakage Volatile and Non-Volatile 7T SRAM Cells”, IETE Journal of Research (Taylor amp; Francis), ISSN: 0377-2063, DOI: 10.1080/03772063.2022.2027279, PP:1-17, Vol:16, Issue:10, Feb-2022.

[3] Hemanth Kumar C S and Kariyappa B S, “Analysis of 7T SRAM Cell Based on MTCMOS, SVL and I-SVL Technique”, Indian Journal of Science and Technology, ISSN: 0974-5645, DOI:10.17485/IJST/v15i23.1991, PP: 1143-1150, Vol:15,Issue: 23, Jun-2022.

[4] H.N. Patel, F.B. Yahya, B.H. Calhoun, Optimizing SRAM bitcell reliability and energy for IoT applications, in: Proc. Int. Symp. on Quality Electronics Design (ISQED), 2016, pp. 12–17

[5] Basavaraj Madiwalar and Dr. Kariyappa B S, “Single Bit-line 7T SRAM cell for Low Power and High SNM” International Multi Conference on Automation, Computing, Control, Communication and Compressed Sensing (IMAC4S-13), Page-223 – 228, 978-1-4673-5089-1,2013, IEEE.

[6] A. Goel, R.K. Sharma, A.K. Gupta, Process variations aware area efficient negative bit-line voltage scheme for improving write ability of SRAM in nanometer technologies, IET Circuits Dev. Syst. 6 (1) (2012) 45

[7] Kariyappa B S, Mr. Basavaraj Madiwalar and et.al,“A Comparative Study of 7T SRAM Cells” International Journal of Computer Trends and Technology (IJCTT) – volume 4 Issue 7, 2231-2803 Page 2188, July 2013.

[8] K. Nose, T. Sakurai, Optimization of VDD and VTH for low-power and high speed applications, Asia South Pacif. Design Automat. Conf (2000) 469–474.
[9] C.B. Kushwah, S.K. Vishvakarma, 'A single-ended with dynamic feedback control 8T subthreshold SRAM cell, IEEE Trans. Very Large Scale Integr. Syst. 24 (1) (2016) 373–377
[10] M.-H. Tu, J.-Y. Lin, M.-C. Tsai, et al., A single-ended disturb-free 9T subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing, IEEE J. Solid State Circuits 47 (6) (2012) 1469– 148
[11] B.H. Calhoun, A.P. Chandrakasan, A 256-kb 65-nm Sub-threshold SRAM design for ultra-low-voltage operation, IEEE J. Solid-State Circuits 42 (3) (2007) 680–688
[12] C.-H. Lo, S.-Y. Huang, P-P-N based 10T SRAM cell for low-leakage and resilient subthreshold operation, IEEE J. Solid-State Circuits 46 (3) (2011) 695–704