

Designing a Pseudo-Random Binary Sequence Generator Using VHDL

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Abstract

The Pseudo Random Binary Sequence (PRBS) generator plays a vital role in various communication systems, cryptography, and testing applications due to its ability to produce sequences that appear random but are deterministically generated. This paper presents the design, implementation, and simulation of a PRBS generator using VHDL (VHSIC Hardware Description Language). The design focuses on linear-feedback shift registers (LFSR) for generating sequences of arbitrary lengths. The PRBS generator's performance is evaluated in terms of sequence length, randomness, and power consumption using standard VHDL simulation tools. The generated sequences are validated for their application in testing, error detection, encryption, and synchronization systems. This study demonstrates how the PRBS generator can be efficiently designed and verified using hardware description languages for use in modern digital systems.

Introduction

Background on Pseudo Random Binary Sequences (PRBS)

A Pseudo-Random Binary Sequence (PRBS) is a sequence of binary values that mimics randomness but is deterministically generated using algorithms. These sequences are used in various applications including testing of communication channels, cryptography, spread spectrum techniques, and digital signal processing. PRBS generators produce repeatable sequences with properties similar to random numbers, making them ideal for performance testing and simulations in systems requiring random-like data patterns.

Importance of PRBS Generators in Digital Systems

PRBS generators are essential in systems that require predictable yet random-like sequences for tasks such as channel testing, system validation, and encryption. These sequences help in assessing the performance of digital systems, measuring error rates, and ensuring system robustness. PRBS is also widely used in pseudo-random noise (PN) sequences, which are important in spread spectrum communications and digital modulation techniques.

Introduction to VHDL

VHDL (VHSIC Hardware Description Language) is a popular hardware description language used to model and simulate digital systems at different levels of abstraction. It is widely used in designing and testing digital circuits, including PRBS generators. VHDL provides a flexible and efficient way to design and implement hardware systems, enabling designers to verify their designs through simulation before proceeding to physical implementation on FPGAs or ASICs.

Objective of the Research

This paper aims to design and simulate a PRBS generator using VHDL. The design uses Linear Feedback Shift Registers (LFSRs) to generate sequences of arbitrary length. The performance of the generator will be analyzed in terms of randomness, sequence length, power consumption, and suitability for practical applications. The results will be validated using simulation tools to ensure that the generated sequences meet the required specifications.

Literature Review

History and Development of PRBS Generators

Pseudo-random binary sequences have been used since the early development of digital communication systems. Early implementations used simple linear feedback shift registers (LFSRs) to generate long sequences of random-like data. PRBS generators have evolved over the years, with more sophisticated algorithms being developed to generate longer sequences with better statistical properties.

PRBS Generators in Modern Digital Systems

Modern digital systems rely heavily on PRBS generators for system validation, encryption, and testing. PRBS sequences are used to stress-test communication systems by simulating random noise and interference. In cryptographic systems, PRBS generators provide random key streams for secure communication. Recent research focuses on optimizing PRBS generators for low power consumption and high-speed applications.

VHDL in Digital Circuit Design

VHDL has become the de facto standard for designing, simulating, and synthesizing digital circuits. The language allows designers to create models that can be simulated at the behavioral, structural, and gate levels, enabling a detailed analysis of the circuit's performance. VHDL also supports the design of complex systems such as PRBS generators, which can be tested under various conditions using simulation tools.

Previous Implementations of PRBS Generators in VHDL

There are several existing studies that detail the implementation of PRBS generators in VHDL. Many of these focus on simple LFSR-based designs, which can be synthesized and implemented on FPGAs or ASICs. Previous research highlights the challenges in optimizing PRBS generators for speed, power efficiency, and sequence length.

Research Gaps

Most existing studies focus on basic LFSR-based PRBS generators. However, there is a lack of research on optimizing these generators for high-performance applications, particularly in the context of modern digital systems that require low power consumption and high throughput. This paper aims to fill this gap by presenting an optimized design of a PRBS generator using VHDL.

Pseudo Random Binary Sequence (PRBS) Generators: Overview and Importance

Theoretical Basis of PRBS Generators

PRBS generators produce a sequence of binary digits (0s and 1s) that appear random but are generated deterministically. The underlying structure is based on Linear Feedback Shift

Registers (LFSRs), which consist of shift registers and feedback logic. The key properties of a PRBS generator are its maximum length sequence, periodicity, and randomness. These properties are critical in applications requiring random-like data patterns.

Linear Feedback Shift Registers (LFSRs)

LFSRs are the building blocks of PRBS generators. They are simple, shift-register circuits with feedback connections that control the sequence generation. The feedback is a linear function of the previous state of the registers, typically implemented using XOR gates. The length of the LFSR determines the period of the generated sequence, while the feedback taps determine the randomness and periodicity of the sequence.

Maximum-Length Sequences

A PRBS generator produces a maximum-length sequence when its feedback polynomial is a primitive polynomial. The maximum sequence length is $2^n - 1$, where n is the number of registers in the LFSR. The sequence repeats itself after this length, making it ideal for applications requiring long pseudo-random sequences.

Characteristics of PRBS Sequences

PRBS sequences exhibit several important characteristics, including balance, run-length distribution, and autocorrelation. These properties make them suitable for applications in cryptography, error detection, and spread spectrum communication.

VHDL Design of PRBS Generator

Overview of VHDL for Digital Circuit Design

VHDL is a robust language for designing digital circuits. It allows designers to describe the behavior of digital systems at various levels of abstraction, from behavioral to structural. VHDL provides the tools necessary to design, simulate, and synthesize PRBS generators.

Design Methodology

The design of the PRBS generator is based on an LFSR architecture. The design involves specifying the number of registers, feedback taps, and the feedback polynomial in VHDL. A structural description of the LFSR is written, where each register and feedback connection is

defined explicitly.

VHDL Code for PRBS Generator

A detailed explanation of the VHDL code for the PRBS generator, including the design of the LFSR, the feedback logic, and the output sequence. The code will be modular, with different components representing the shift registers and feedback logic. Special attention is given to the feedback polynomial, which determines the maximum-length sequence.

Testing and Verification of the VHDL Code

The design is tested using VHDL simulation tools. The simulation verifies that the PRBS generator produces the expected pseudo-random sequence. Different test cases are used to verify the correctness of the design, including tests for maximum sequence length, periodicity, and randomness.

Simulation and Implementation

Simulation Tools and Environment

The simulation is performed using tools such as ModelSim or Vivado. These tools provide a platform for verifying the functionality of the PRBS generator in a controlled environment. The simulation setup, including clock speed, input parameters, and expected outputs, is discussed in detail.

Simulation Results for PRBS Generator

The simulation results are presented in terms of the output sequences generated by the PRBS generator. The randomness of the sequences is verified by comparing the generated sequences with theoretical expectations. Waveforms and sequence tables are provided to illustrate the correct operation of the generator.

Synthesis of the PRBS Generator on FPGA

After simulation, the PRBS generator is synthesized on an FPGA. The synthesis process involves mapping the VHDL design to the hardware resources of the FPGA. The performance of the PRBS generator on the FPGA is analyzed in terms of resource utilization, speed, and power consumption.

Applications of PRBS Generators in Modern Systems

PRBS Generators in Communication Systems

PRBS generators are widely used in communication systems for error detection, synchronization, and channel testing. This section explores how PRBS sequences are used in testing communication channels for noise and interference resilience. Examples include their use in LTE, 5G, and spread spectrum communication systems.

Cryptography and Encryption

In cryptography, PRBS generators provide random key streams for encryption algorithms. The security of these algorithms depends on the unpredictability of the PRBS sequences. This section discusses how PRBS generators are used in stream ciphers and other cryptographic systems.

PRBS in Testing and Validation of Digital Systems

PRBS generators are used extensively in testing digital systems for robustness against errors and noise. This section provides examples of how PRBS sequences are used in built-in self-test (BIST) systems, error-detection circuits, and system validation.

Conclusion

The design and simulation of a PRBS generator using VHDL demonstrate the effectiveness of hardware description languages in digital circuit design. The PRBS generator provides a reliable method for generating random-like sequences that are useful in a variety of applications. The performance of the PRBS generator was verified through simulation, and the results confirmed that the generator meets the required specifications for sequence length, randomness, and efficiency. Future work could focus on optimizing the design for low-power applications or extending the design to support more complex feedback polynomials for enhanced randomness.

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